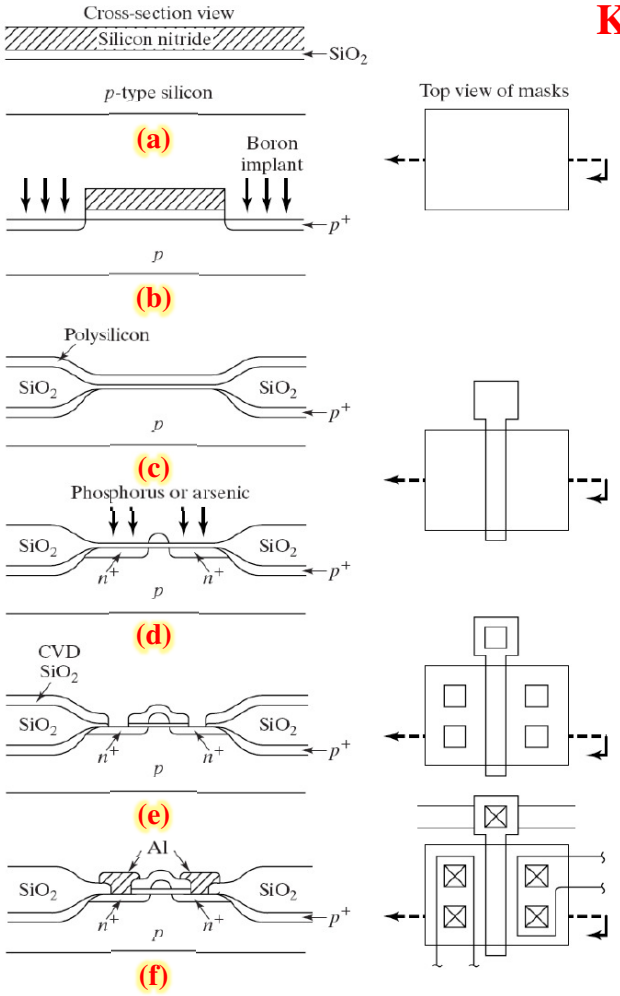
반도체 공정 이론 교육
(기초 과정)

부산대학교
반도체공동연구소

Introduction:
Basic N-MOSFET Process Sequence

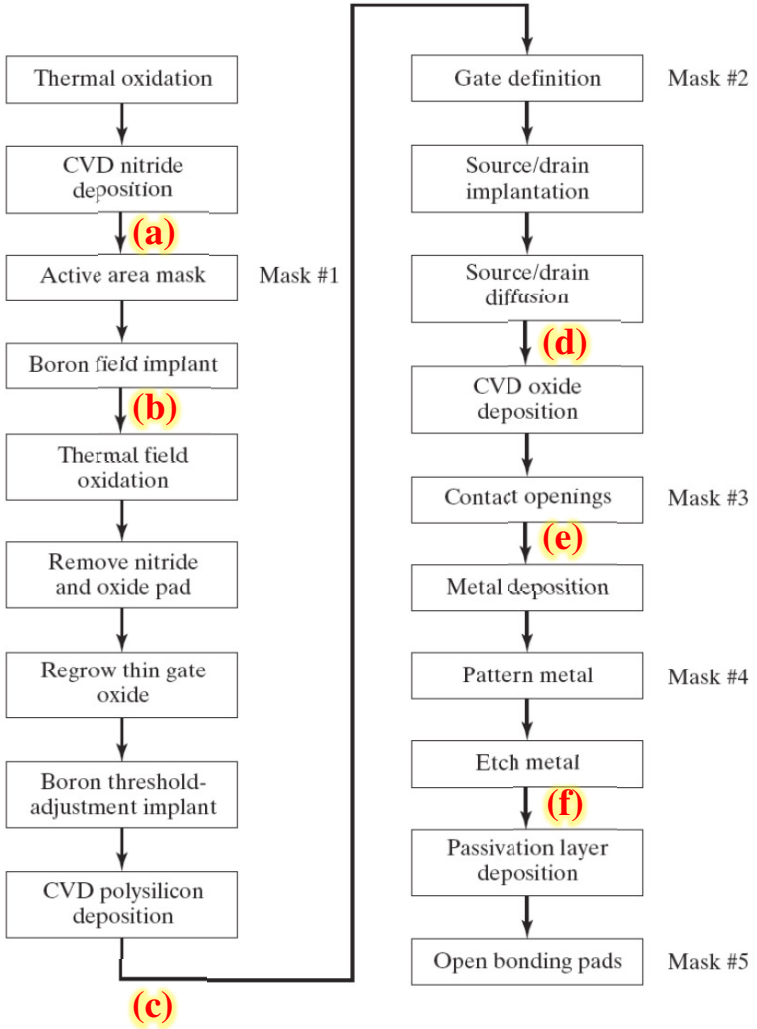


Key Elementary Process

- Oxidation
- Photolithography
- Implantation
- Diffusion
- Etching
- Film Deposition

FIGURE 1.6

Process sequence for a semirecessed oxide NMOS process. (a) Silicon wafer covered with silicon nitride over a thin padding layer of silicon dioxide; (b) etched wafer after first mask step. A boron implant is used to help control field oxide threshold; (c) structure following oxidation, nitride removal, and polysilicon deposition; (d) wafer after second mask step and etching of polysilicon; (e) the third mask has been used to open contact windows following silicon dioxide deposition; (f) final structure following metal deposition and patterning with fourth mask.

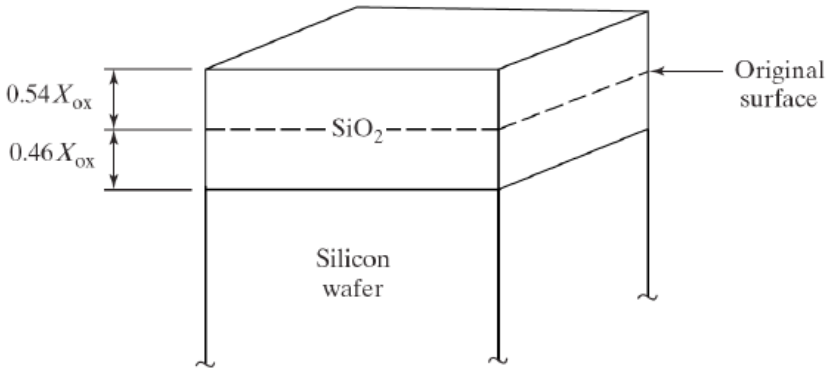


Part 1.
Details of Processes

1.Oxidation
2.Photo-Lithography
3.Ion-Implantation
4.Diffusion
5.Etching
6.Film Deposition

1. Oxidation: Thermal Oxidation of Silicon

- Silicon Dioxide
  - High quality electrical insulator
  - Diffusion/implantation barrier
  - Passivates silicon surface



Dry Oxidation

$$S_i + O_2 \rightarrow S_iO_2$$

Wet Oxidation

$$S_i + 2H_2O \rightarrow S_iO_2 + 2H_2$$

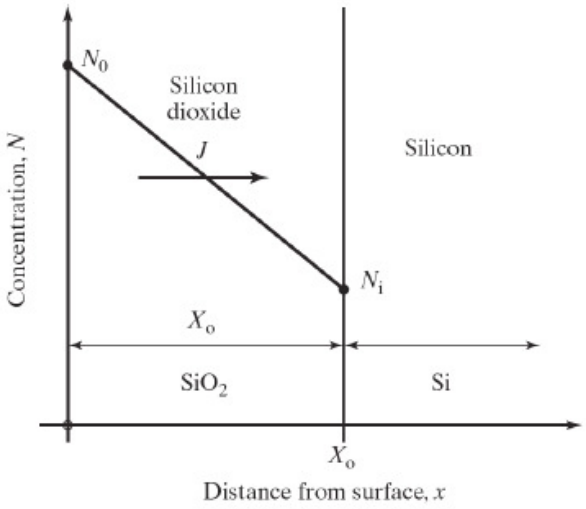
Growth Occurs 54% above and 46% below original surface as silicon is consumed

1. Oxidation: Fick's First Law of Diffusion

Particle flux J is proportional to the negative of the gradient of the particle concentration

$$J = -D\frac{\partial N}{\partial x}$$ D = diffusion coefficient

Particles move from a region of high concentration to one of low concentration



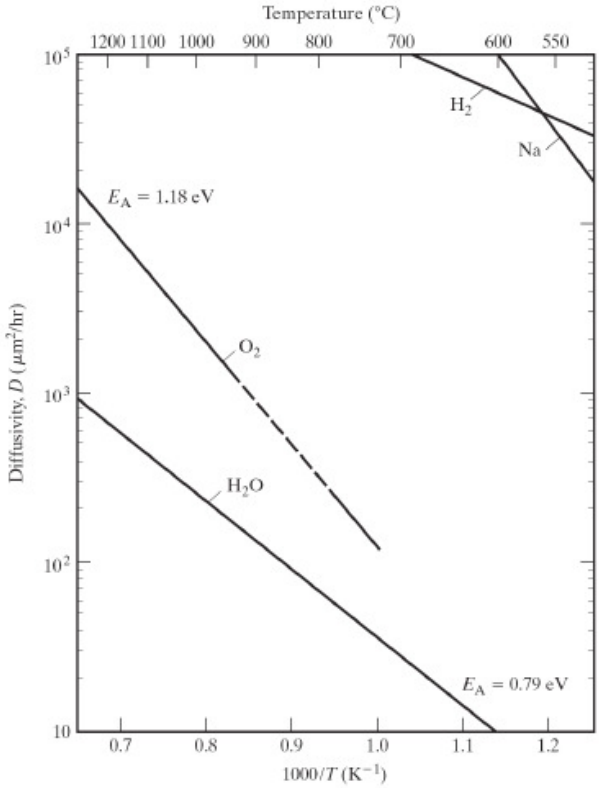


FIGURE 3.1

Diffusivities of hydrogen, oxygen, sodium, and water vapor in silicon glass. Copyright John Wiley & Sons, Inc. Reprinted with permission from Ref. [4].

1. Oxidation: Local Oxidation of Silicon (LOCOS) to isolate MOSFETs

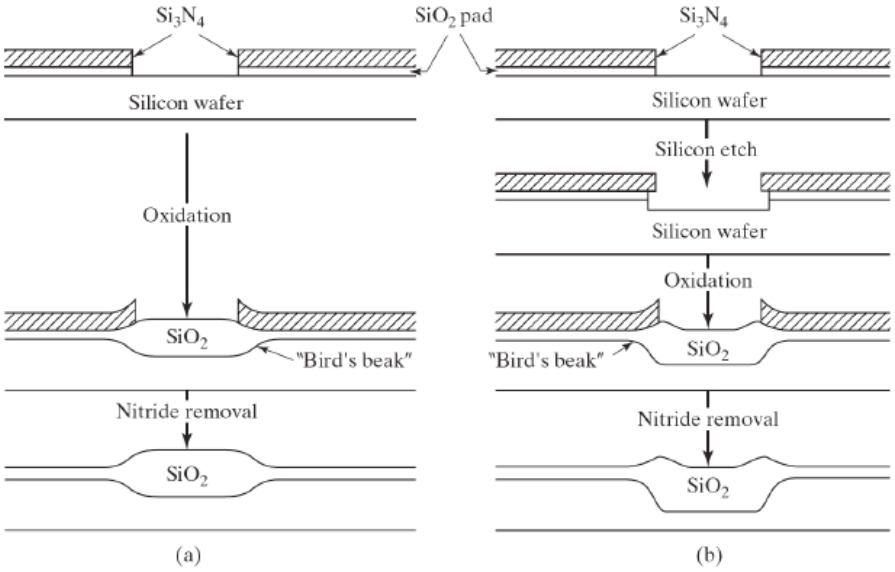
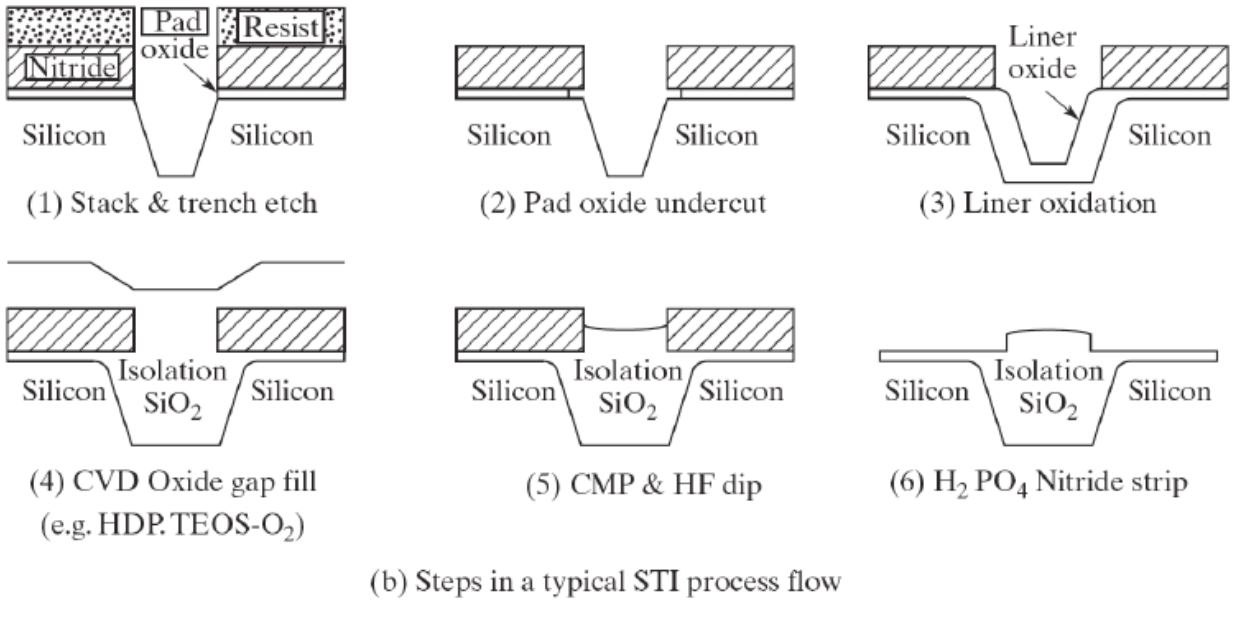


FIGURE 3.12

Cross section depicting process sequence for local oxidation of silicon (LOCOS): (a) semirecessed and (b) fully recessed structures.

- Isolation technology in MOS processes
- Provides isolation between nearby devices
- Fully recessed process attempts to minimize bird's beak

1. Oxidation: Shallow Trench Isolation (STI) for minimizing the MOSFET pitch

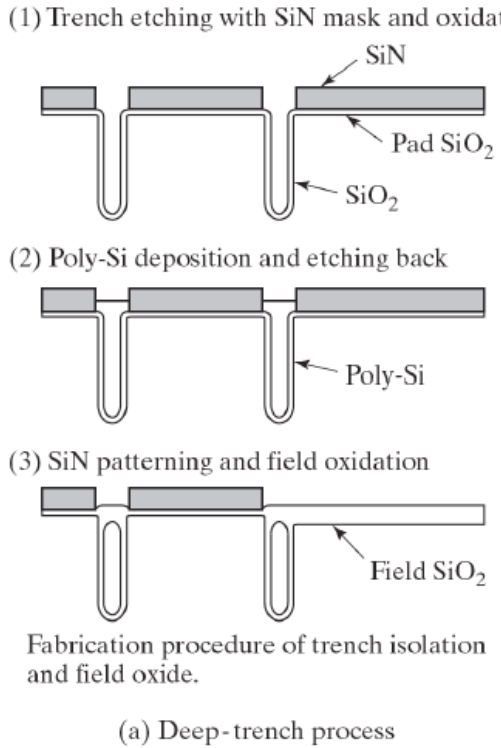


Used for isolation between devices and to minimize device capacitance

FIGURE 3.13

Trench isolation structures. (a) Deep trench isolation - Copyright 1996 IEEE. Reprinted with permission from Ref. [18]. (b) Shallow trench isolation - Copyright 1998 IEEE. Reprinted with permission from Ref. [20].

1. Oxidation: Deep Trench Isolation (DTI) for further minimizing the MOSFET pitch



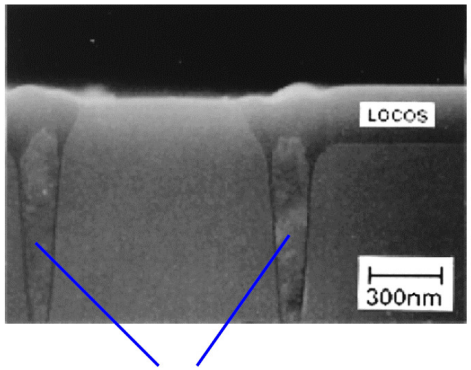
Fabrication procedure of trench isolation and field oxide.

(a) Deep-trench process

FIGURE 3.13

Trench isolation structures. (a) Deep trench isolation - Copyright 1996 IEEE. Reprinted with permission from Ref. [18]. (b) Shallow trench isolation - Copyright 1998 IEEE. Reprinted with permission from Ref. [20].

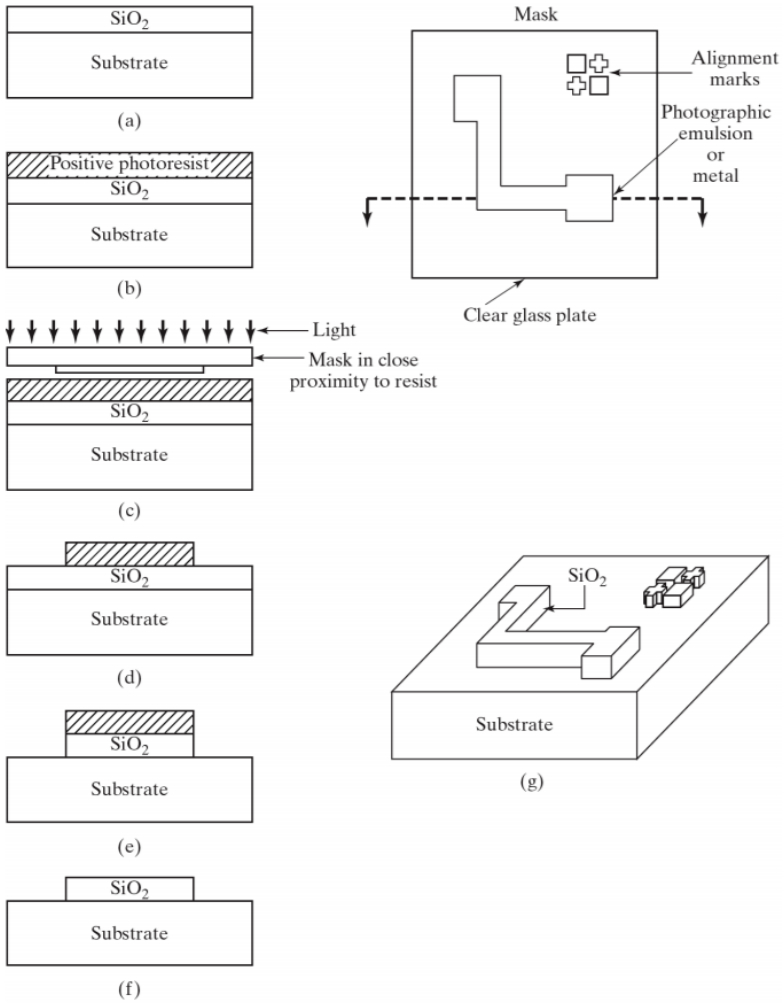
- Often used in dynamic memory chips (DRAMS)
- Deep trenches used in high performance bipolar processes



Filled Trenches

2. Photo-Lithography:

Example to form SiO_2 island



(a) Substrate covered with silicon dioxide barrier layer

(b) Positive photoresist applied to wafer surface

(c) Mask in close proximity to surface

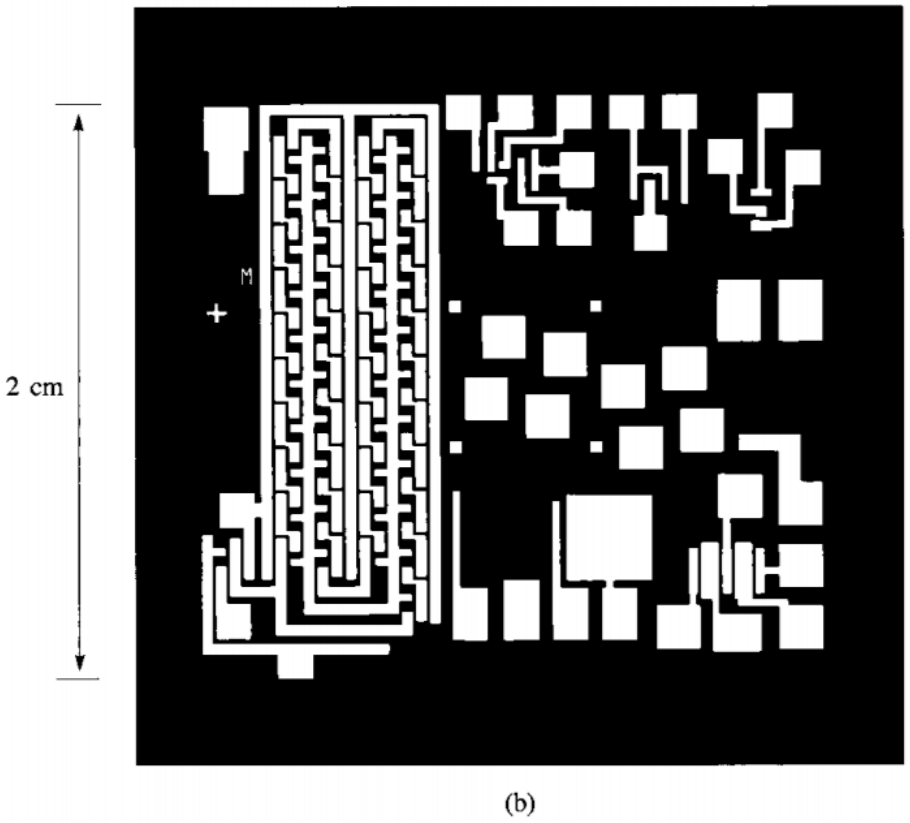
(d) Substrate following resist exposure and development

(e) Substrate after etching of oxide layer

(f) Oxide barrier on surface after resist removal

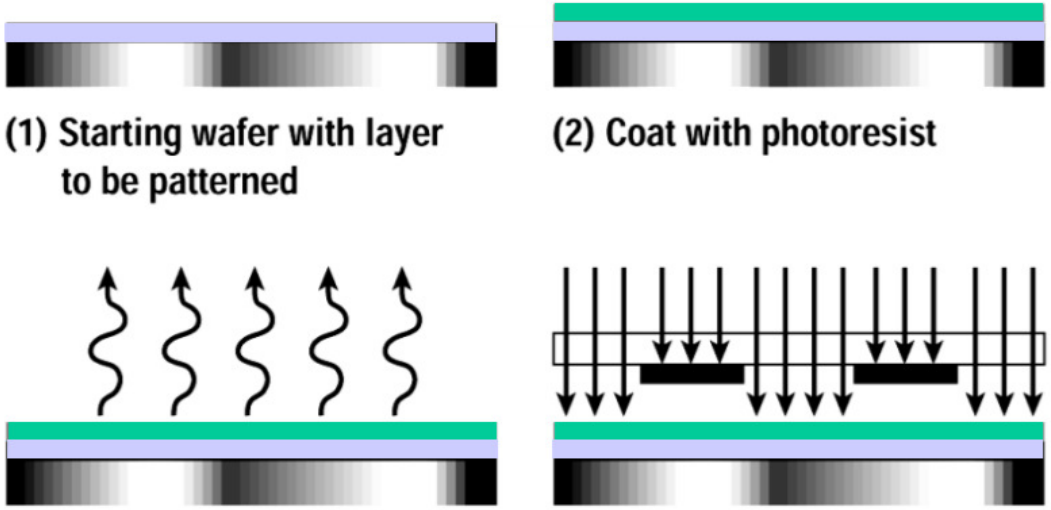
(g) View of substrate with silicon dioxide pattern on the surface

2. Photo-Lithography: Mask (example)



- Example of 10X reticle for the metal mask - this particular mask is ten times final size (10 μm minimum feature size - huge!)
- Used in step-and-repeat operation
- One mask for each lithography level in process

2. Photo-Lithography: Process Sequence



(1) Starting wafer with layer to be patterned

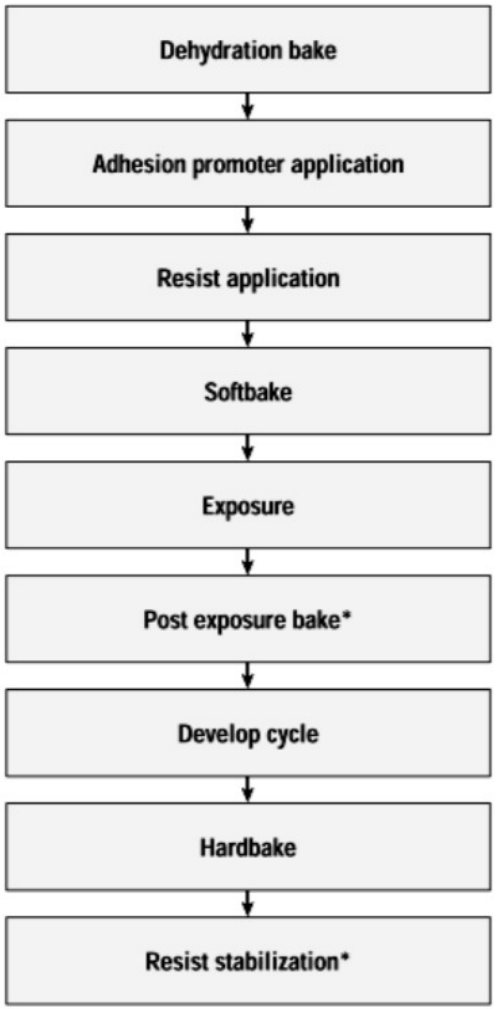
(2) Coat with photoresist

(3) Bake the resist to set its dissolution properties

(4) Expose resist by shining light through a photomask

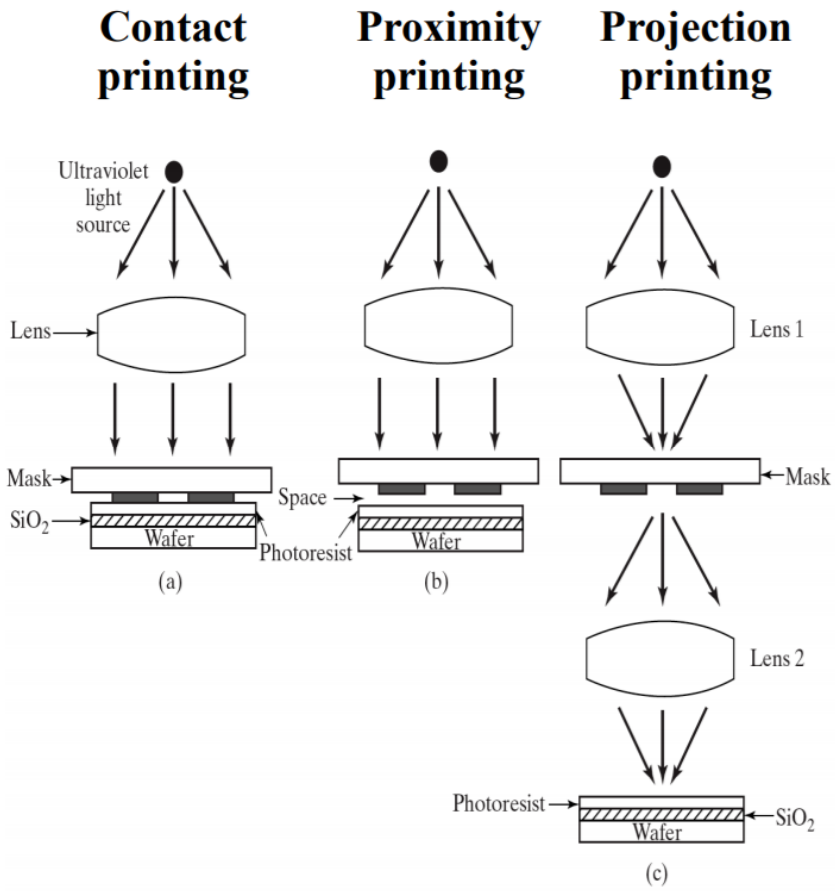
(5) Immerse exposed wafer in developer

(6) Etch the film



*Optional steps

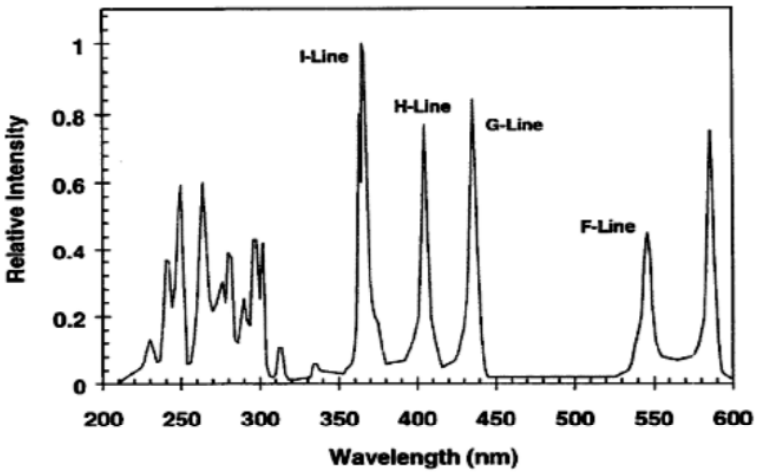
2. Photo-Lithography: Related Optics



- Contact printing damages the mask and the wafer and limits the number of times the mask can be used
- Proximity printing eliminates damage
- Projection printing can operate in reduction mode with direct step-on-wafer

2. Photo-Lithography: Optical Source

- Hg Arc lamps 436(G-line), 405(H-line), 365(I-line) nm



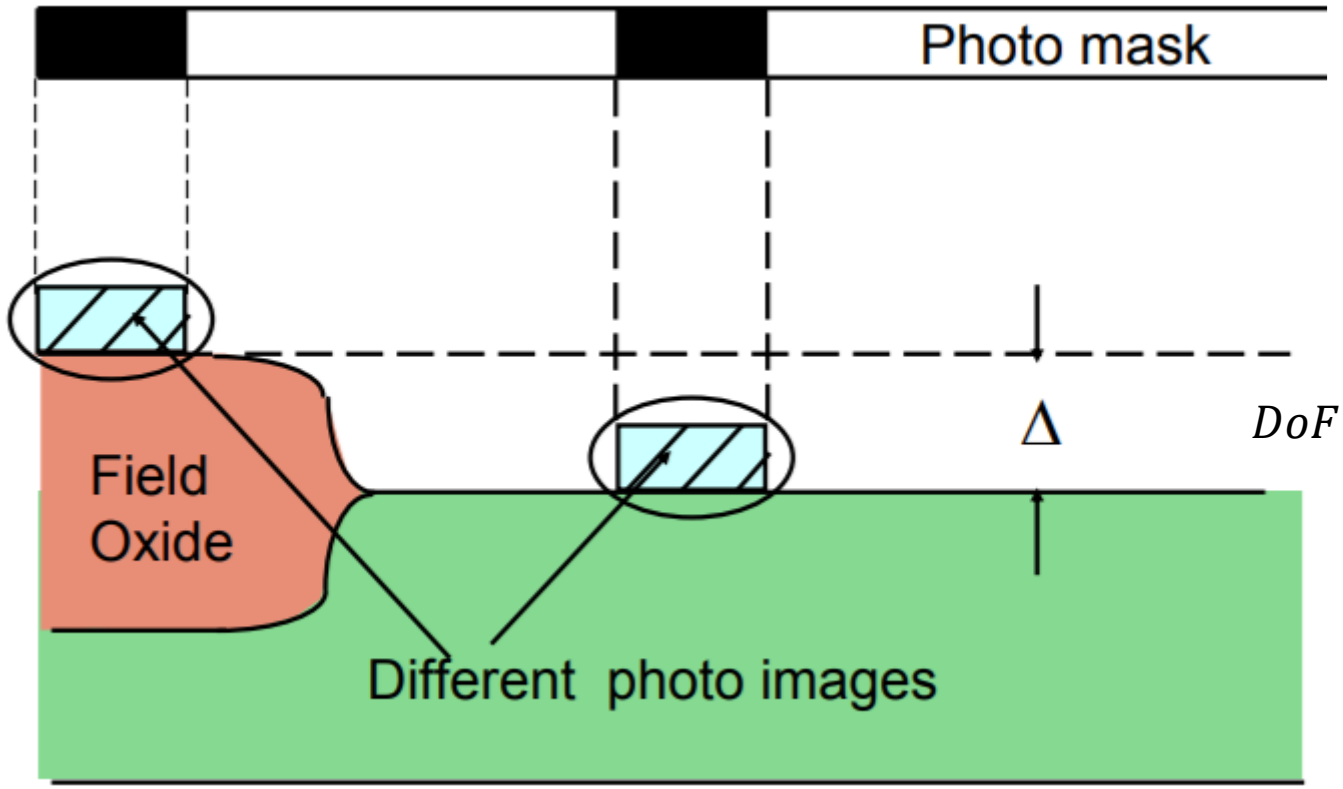
$$F = 0.5\frac{\lambda}{\sin\theta_c}$$

Trade-off

$$DoF = 0.6\frac{\lambda}{(\sin\theta_c)^2}$$

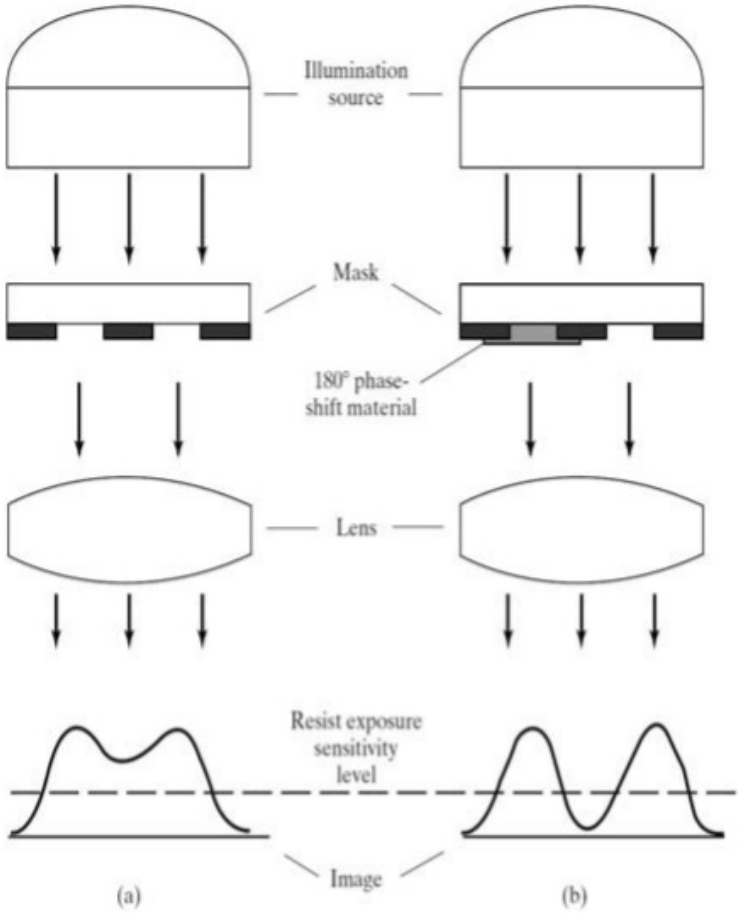
- Excimer lasers: KrF (248nm) and ArF (193nm)
- Laser pulsed plasma (13nm, EUV)
- Source Monitoring
  - Filters can be used to limit exposure wavelengths
  - Intensity uniformity has to be better than several % over the collection area
  - Needs spectral exposure meter for routine calibration due to aging

2. Photo-Lithography: Example of DoF Problem



$$DoF = 0.6\frac{\lambda}{(\sin\theta_c)^2}$$

2. Photo-Lithography: Sub-resolution issue and Phase shifting mask

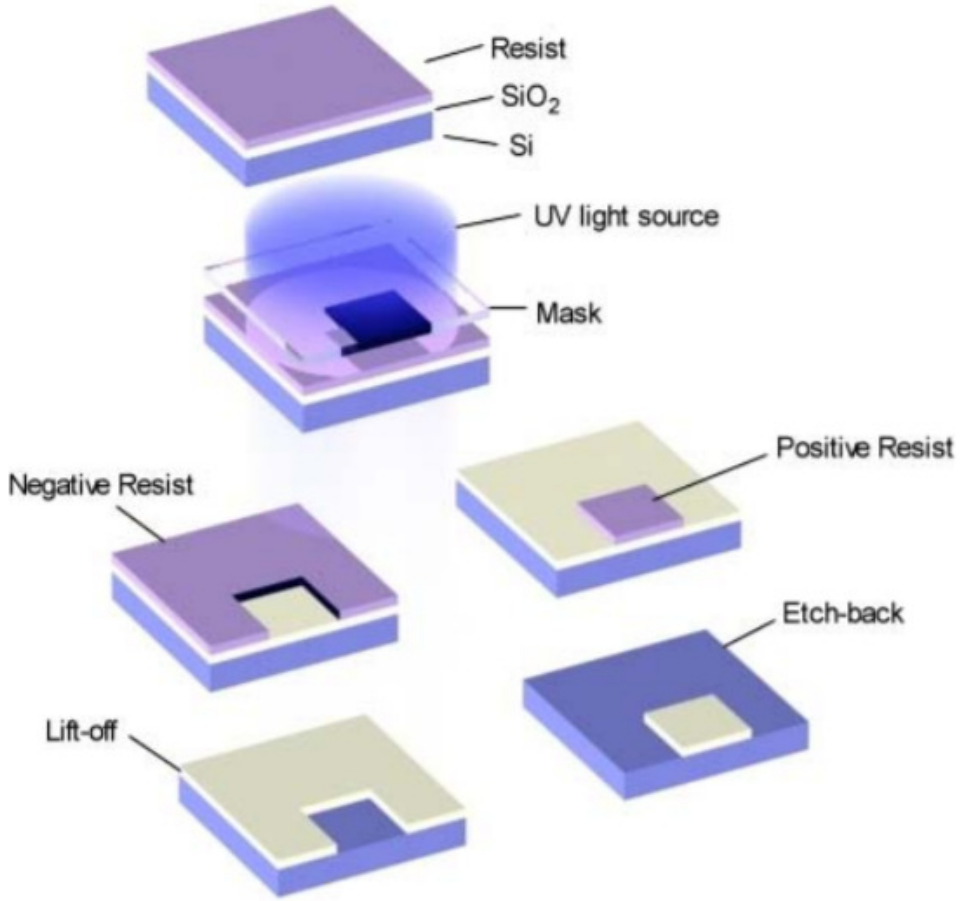


Pattern transfer of two closely spaced lines

(a) Conventional mask technology - lines not resolved

(b) Lines can be resolved with phase-shift technology

2. Photo-Lithography: Etching and Photoresist

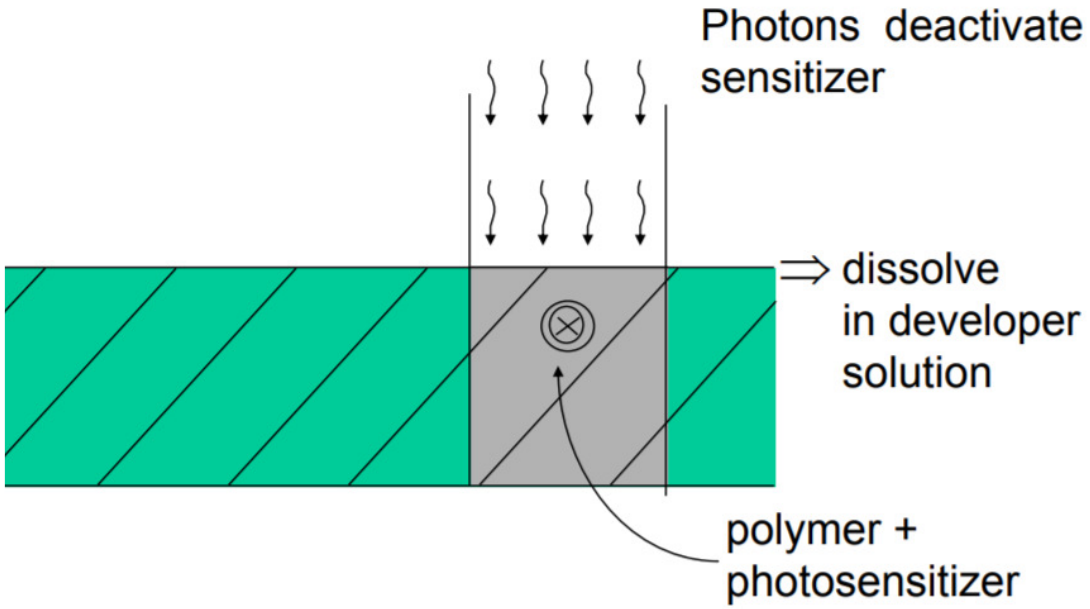


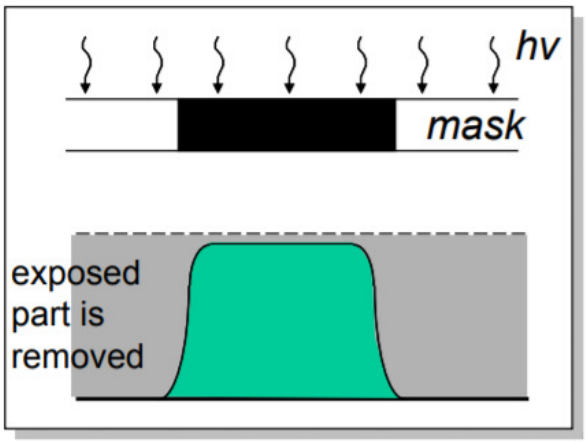
- Resists
  - Positive
  - Negative
- Exposure Sources
  - Light
  - Electron beams
  - Xray sensitive

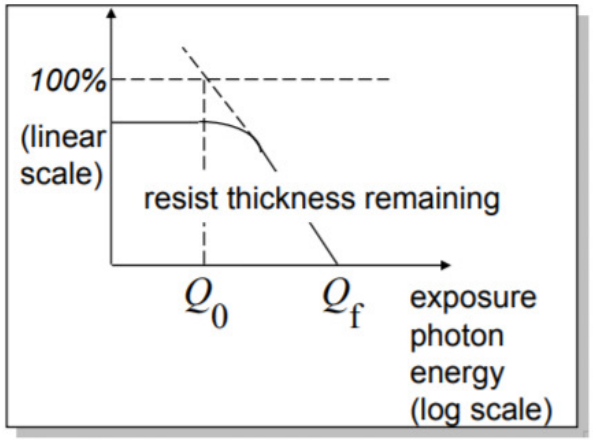
2. Photo-Lithography: Photoresist types

- Negative Resist
  - Composition:
    - Polymer (Molecular Weight (MW) ~65000)
    - Light Sensitive Additive: Promotes Crosslinking
    - Volatile Solvents
  - Light breaks N-N in light sensitive additive => Crosslink Chains
  - Sensitive, hard, Swelling during Develop
- Positive Resist
  - Composition
    - Polymer (MW~5000)
    - Photoactive Dissolution Inhibitor (20%)
    - Volatile Solvents
  - Inhibitor Looses N_2 => Alkali Soluble Acid
  - Develops by “etching” - No Swelling.

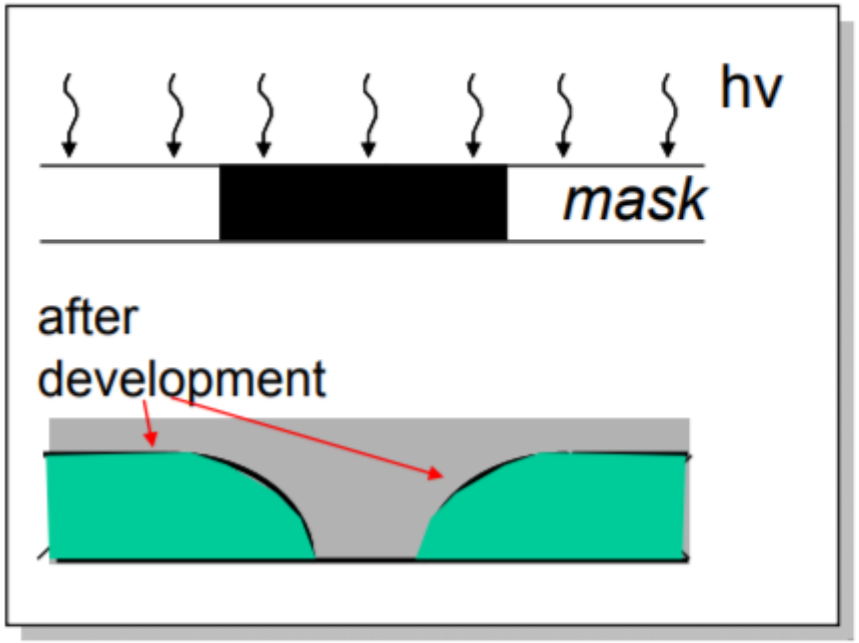
2. Photo-Lithography: Positive PR mechanisms

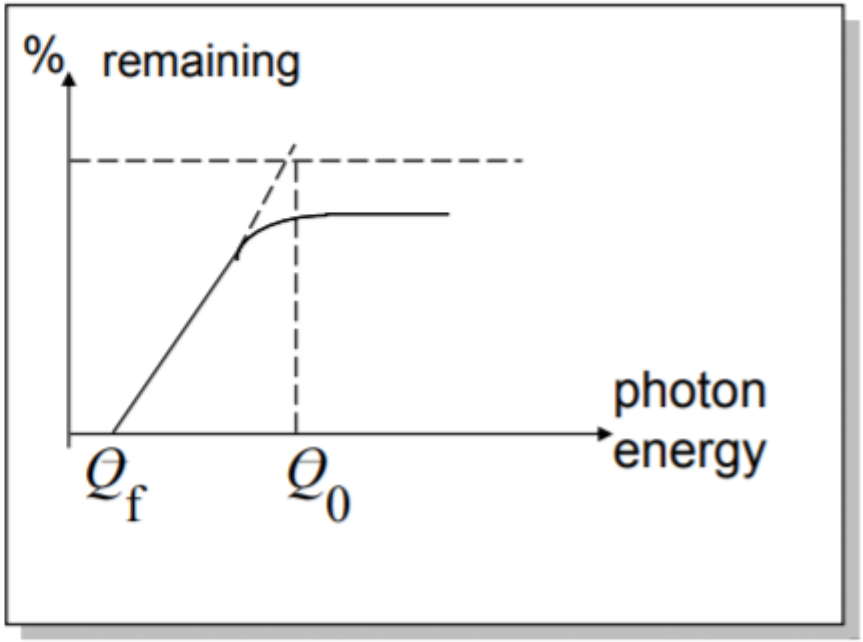






2. Photo-Lithography: Negative PR mechanisms





hv => cross-linking => insoluble in developer solution.

3. Ion-Implantation: Set-up

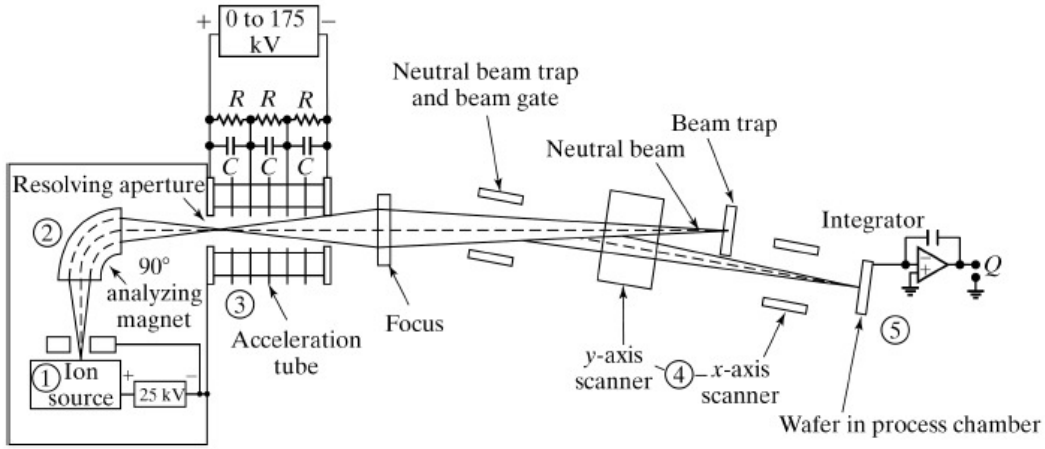


FIGURE 5.1

Schematic drawing of a typical ion implanter

1. Ion Source
2. Mass Spectrometer
3. High-Voltage Accelerator (Up to 5 MeV)
4. Scanning System
5. Target Chamber

Force on charged particle $\vec{F} = q(\vec{v} \times \vec{B})$

Magnetic Field $|\vec{B}| = \sqrt{\frac{2mV}{qr^2}}$

Implanted Dose $Q = \frac{1}{mqA}\int_0^T I(t)dt$

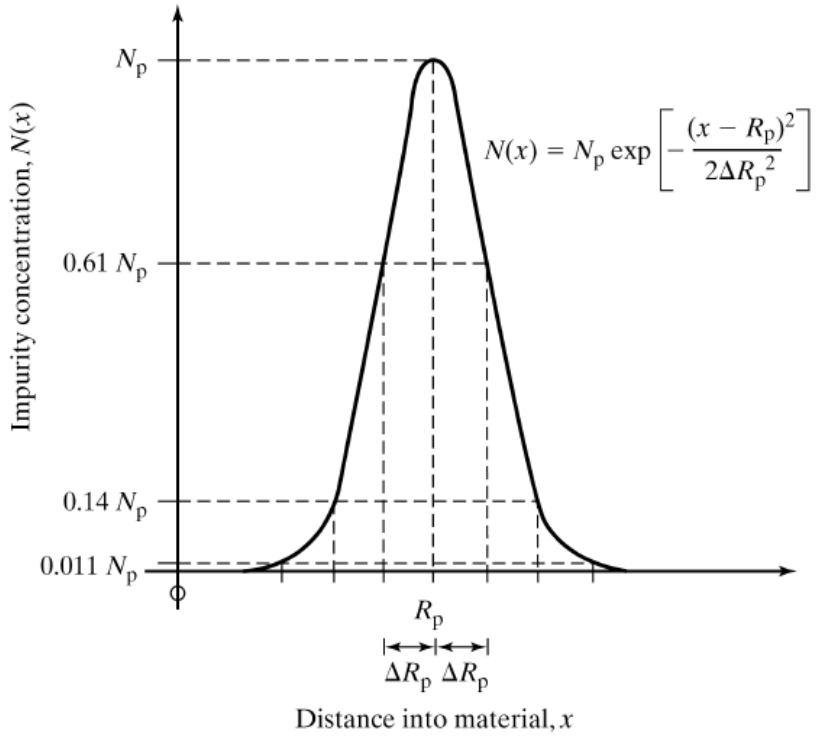
m = mass

$\vec{v}$ = velocity

V = acceleration potential

A = wafer area

3. Ion-Implantation: Mathematical Model



Gaussian Profile

$$N(x) = N_p \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right]$$

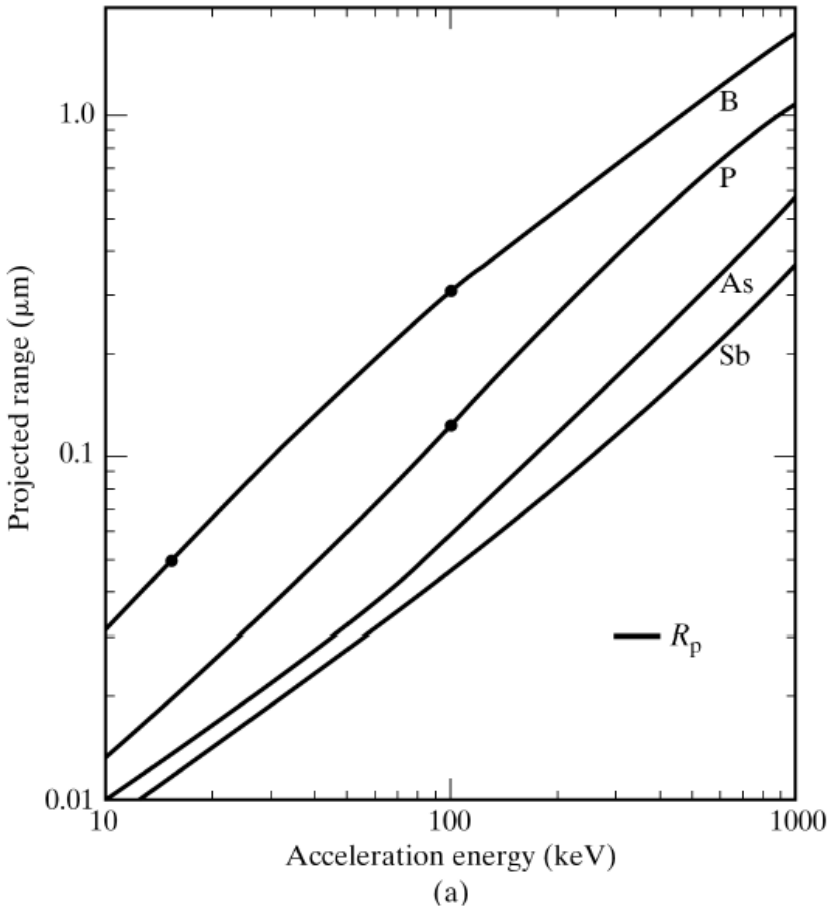
R_p = Projected Range

ΔR_p = Straggle

Dose $$Q = \int_0^\infty N(x)dx = \sqrt{2\pi} N_p \Delta R_p$$

Further reading (my paper): http://210.101.116.15/kiss5/viewer.asp

3. Ion-Implantation: Projected Range



Projected Range:
Implanted depth
←Deeper
as a lighter one

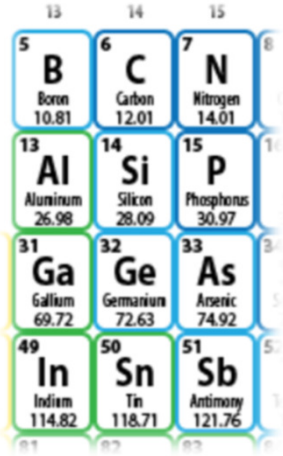
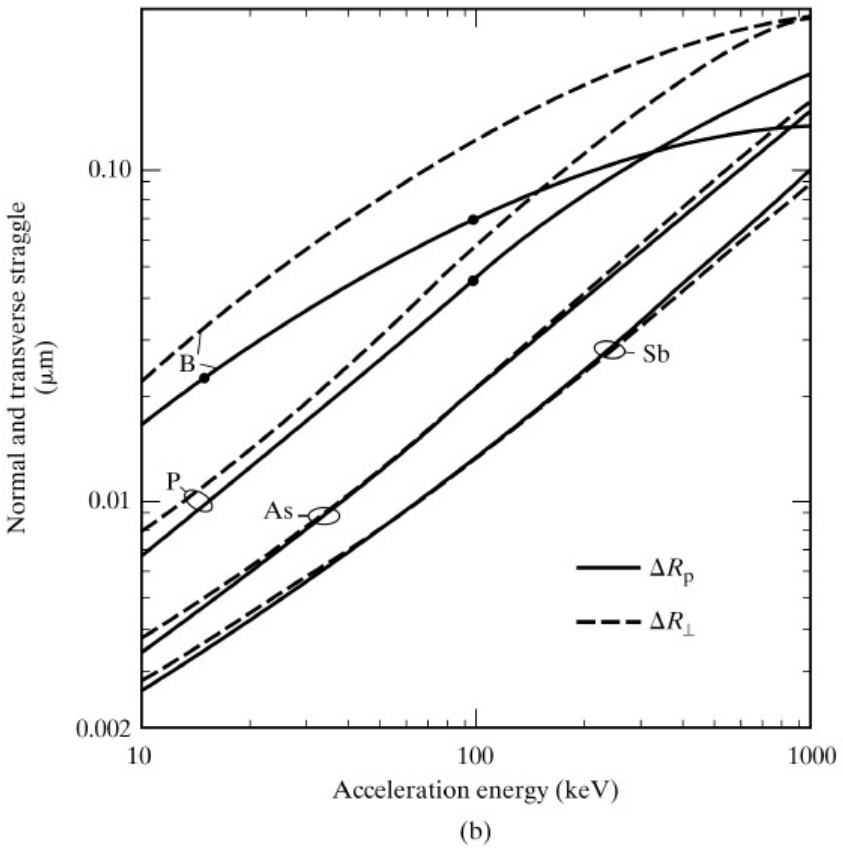


FIGURE 5.3

Projected range and straggle calculations based on LSS theory. (a) Projected range R_p for boron, phosphorus, arsenic, and antimony in amorphous silicon. Results for SiO_2 and for silicon are virtually identical. (b) Vertical ΔR_p and transverse ΔR_l straggle for boron, phosphorus, arsenic, and antimony. Reprinted with permission from Ref. [2]. (Copyright van Nostrand Reinhold Company, Inc.)

3. Ion-Implantation: Straggle



Straggle:
Spreading width
←Wider
as a lighter one

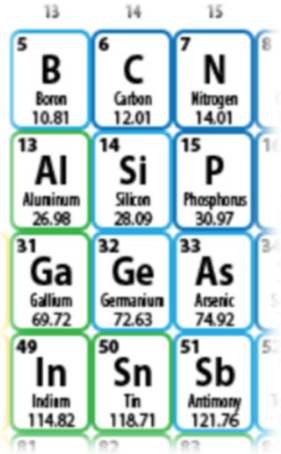
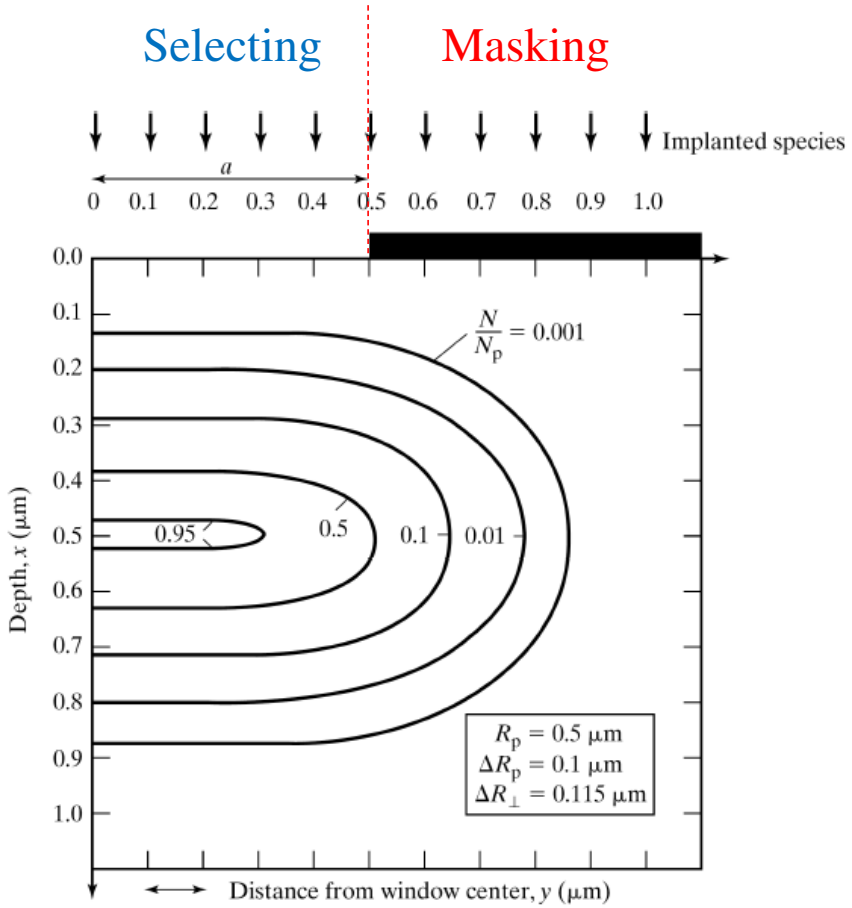


FIGURE 5.3

Projected range and straggle calculations based on LSS theory. (a) Projected range $R_{p\_}$ for boron, phosphorus, arsenic, and antimony in amorphous silicon. Results for SiO_2 and for silicon are virtually identical. (b) Vertical $\_R_p$ and transverse $\_R_l$ straggle for boron, phosphorus, arsenic, and antimony. Reprinted with permission from Ref. [2]. (Copyright van Nostrand Reinhold Company, Inc.)

3. Ion-Implantation: Selecting and Masking



$$N(x,y) = N(x)F(y)$$

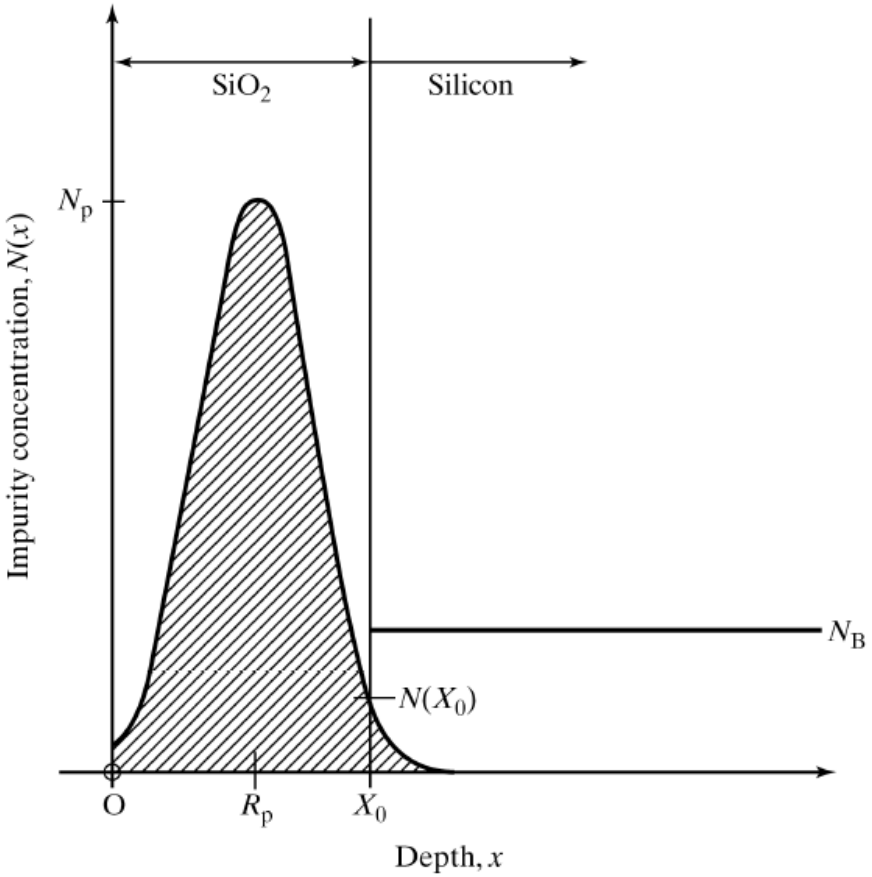
$$F(y) = \frac{1}{2}\left[erfc\left(\frac{y-a}{\sqrt{2}\Delta R_{\perp}}\right) - erfc\left(\frac{y+a}{\sqrt{2}\Delta R_{\perp}}\right)\right]$$

$\Delta R_{\perp}$ = transverse straggle

N(x) is one - dimensional solution

Figure 5.4
Contours of equal ion concentration for an implantation into silicon through a 1-μm window. The profiles are symmetrical about the x-axis and were calculated using the equation above taken from Ref. [3].

3. Ion-Implantation: Masking



- Desire Implanted Impurity Level to be Much Less Than Wafer Doping

$$N(X_0) << N_B$$

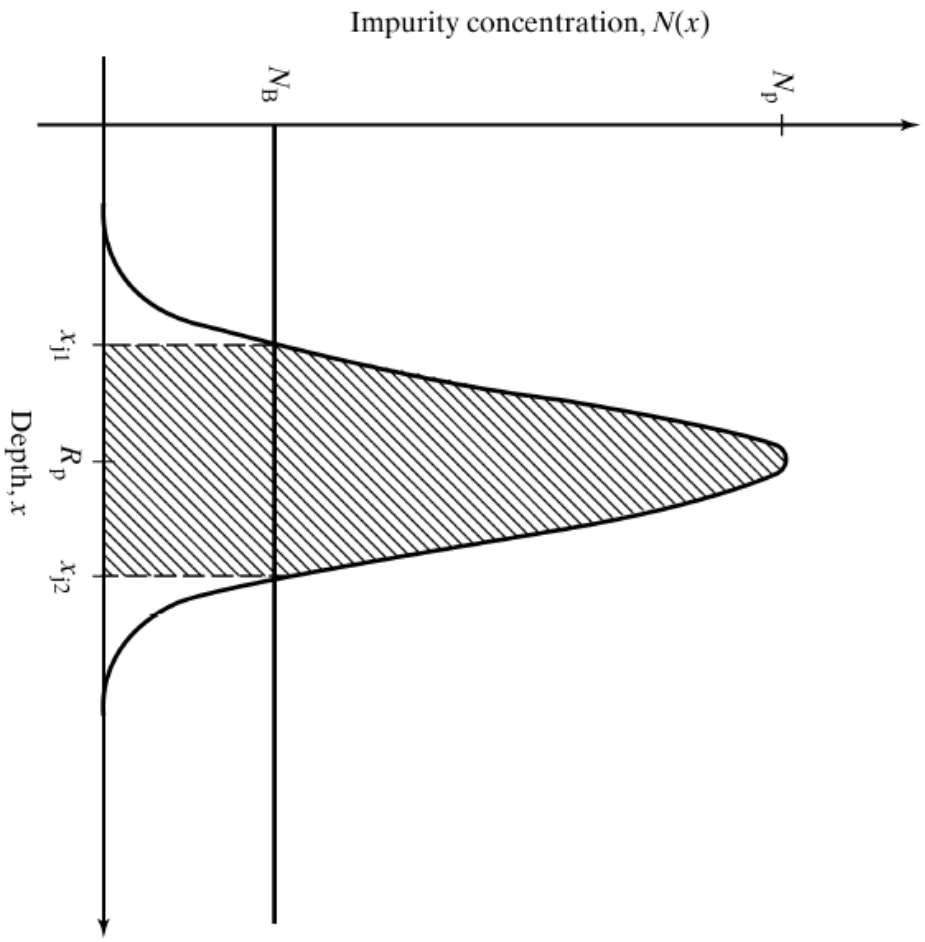
or

$$N(X_0) < N_B/10$$

FIGURE 5.5

Implanted impurity profile with implant peak in the oxide. The barrier material must be thick enough to ensure that the concentration in the tail of the distribution is much less than N_B.

3. Ion-Implantation: Junctions



$$N(x_j) = N_B$$

$$N_p \exp\left[-\frac{(x_j - R_p)^2}{2\Delta R_p^2}\right] = N_B$$

$$x_j = R_p \pm \Delta R_p \sqrt{2\ln\left(\frac{N_p}{N_B}\right)}$$

FIGURE 5.6

Junction formation by impurity implantation in silicon. Two *pn* junctions are formed at x_{j1} and x_{j2}.

3. Ion-Implantation: Channeling

Channeling: Dependence on implantation angle

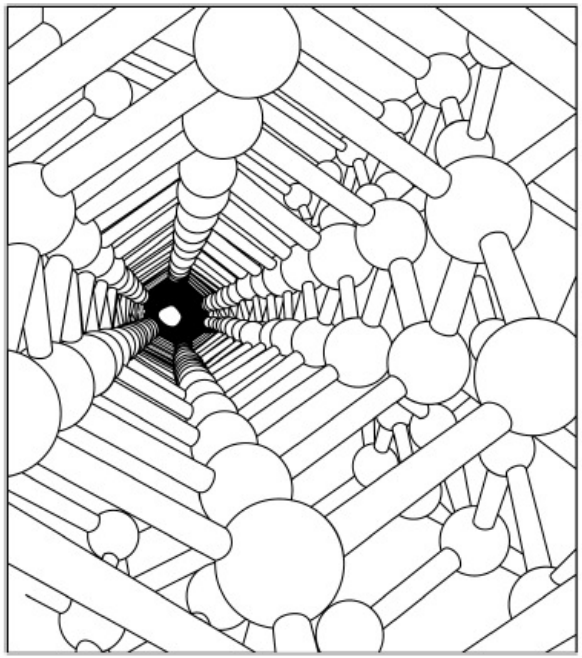


FIGURE 5.7

The silicon lattice viewed along the {110} axis. From THE ARCHITECTURE OF MOLECULES by Linus Pauling and Roger Hayward. Copyright © 1964 W. H. Freeman and Company. Reprinted with permission from Refs. [4a] and [4b].

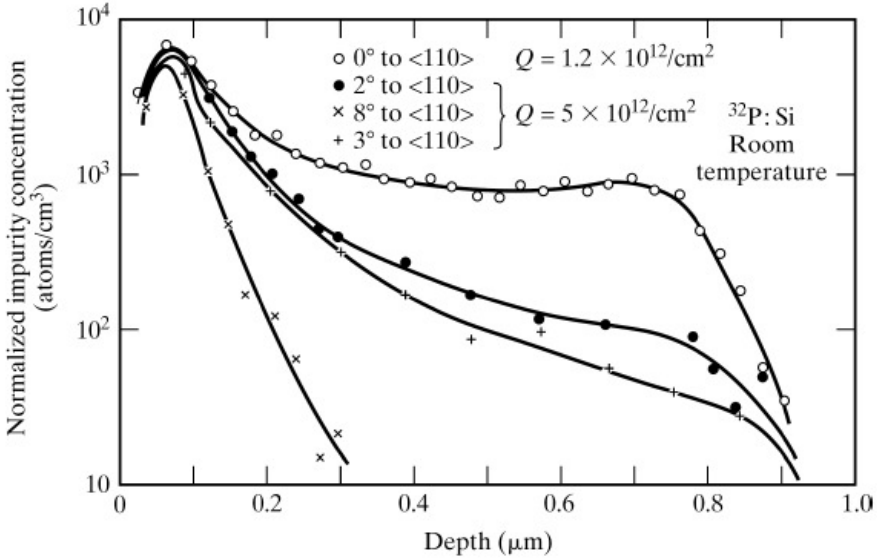
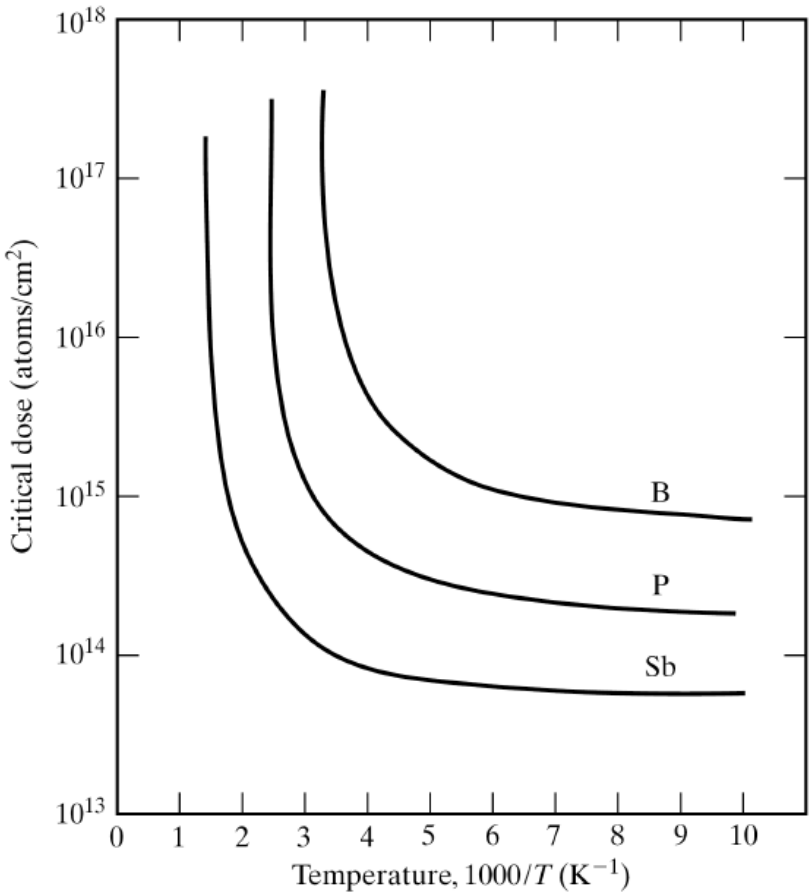


FIGURE 5.8

Phosphorus impurity profiles for 40-keV implantations at various angles from the axis. Copyright 1968 by national Research Council of Canada. Reprinted with permission from Ref. [5].

3. Ion-Implantation: Lattice Damage

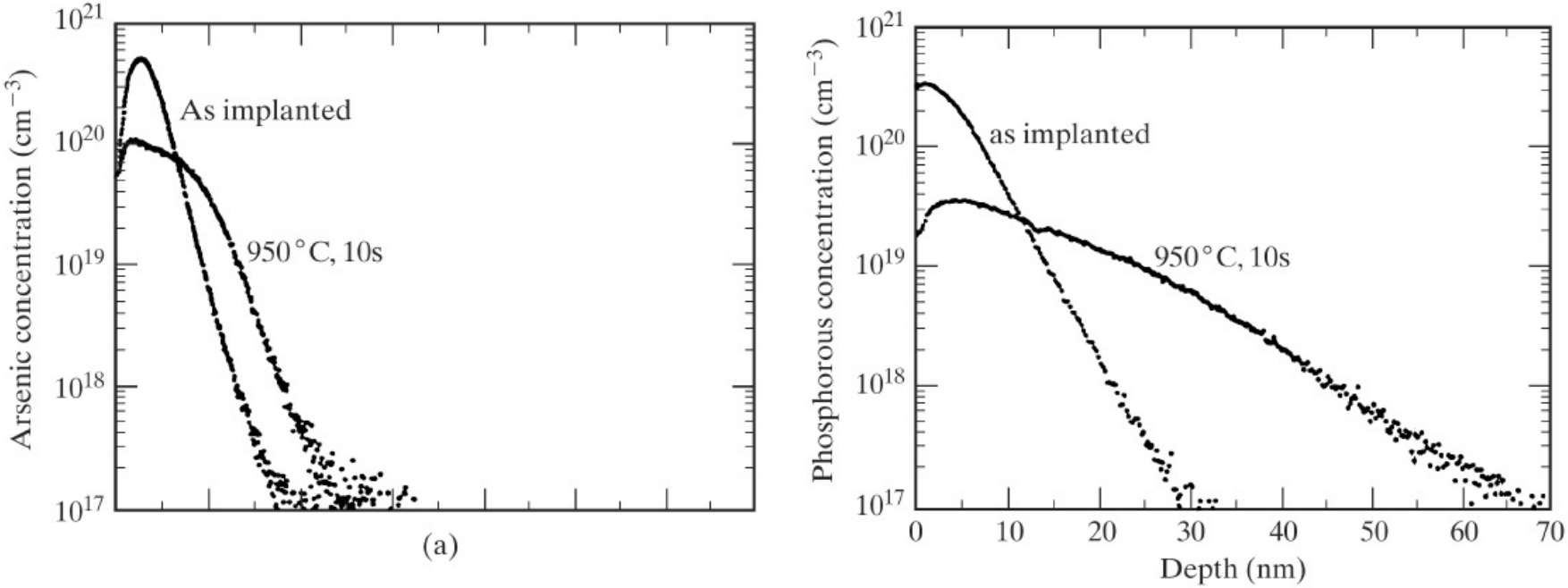


- Implantation Causes Damage to Surface
- Typically Removed by Annealing Cycle 800-1000° C for 30 min.
- Rapid Thermal Annealing (RTA) Now Used for Lower Dt Product

FIGURE 5.9

A plot of the dose required to form an amorphous layer on silicon versus reciprocal target temperature. Arsenic falls between phosphorus and antimony. Copyright 1970 by Plenum Publishing Corporation. Reprinted with permission from Ref. [6].

3. Ion-Implantation: Typical Annealing to recover the damage, and issue

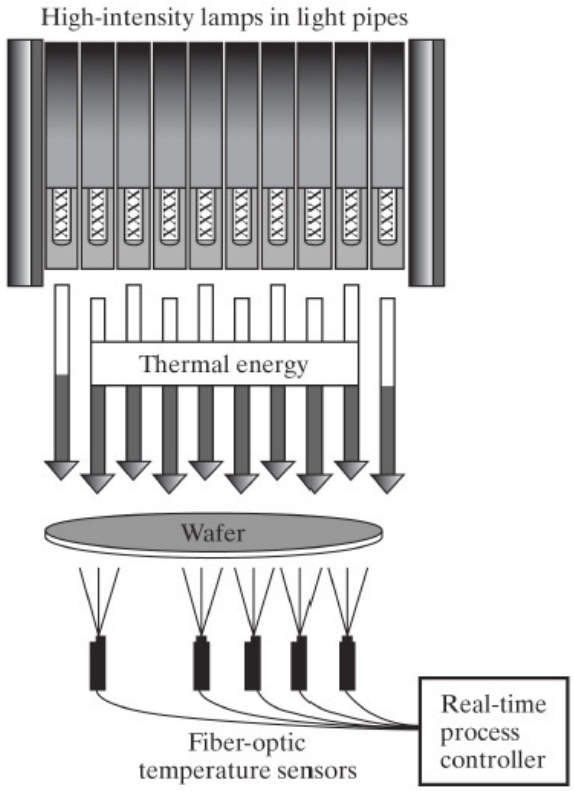


D*t product is high → spreaded

FIGURE 5.11

Examples of transient enhanced diffusion. SIMS data comparing as-implanted and annealed depth profiles from (a) 3 x 10^{14}/cm^2, 2 keV As$^+$, and (b) 3 x 10^{14}/cm^2, 1 keV P$^+$. Annealing conditions were 950°C for 10 sec. SIMS depth profiles of 1 x 10^{15}/cm^2 B implanted at 0.5-, 1-, 2-, and 5 keV (c) as-implanted, and (d) after annealing at 1050°C for 10 sec. Copyright 1997 IEEE. Reprinted with permission from Ref. [13].

3. Ion-Implantation: RTA (Rapid Thermal Annealing)



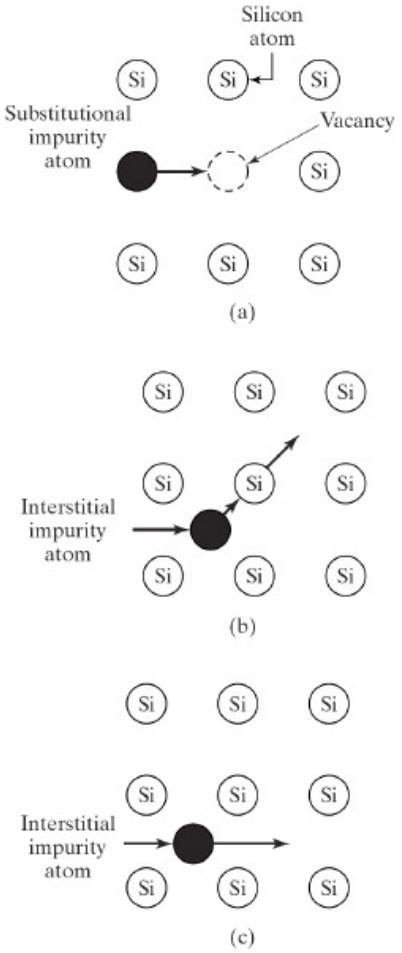
(a)

- Rapid Heating
- 950-1050° C
- 50° C/sec
- Very Low Dt

(b)

Figure 5.12
(a) Concept for a rapid thermal annealing (RTP) system. (b) Applied Materials 300 mm RTP System (Courtesy Applied Materials)

4. Diffusion Process: Overview

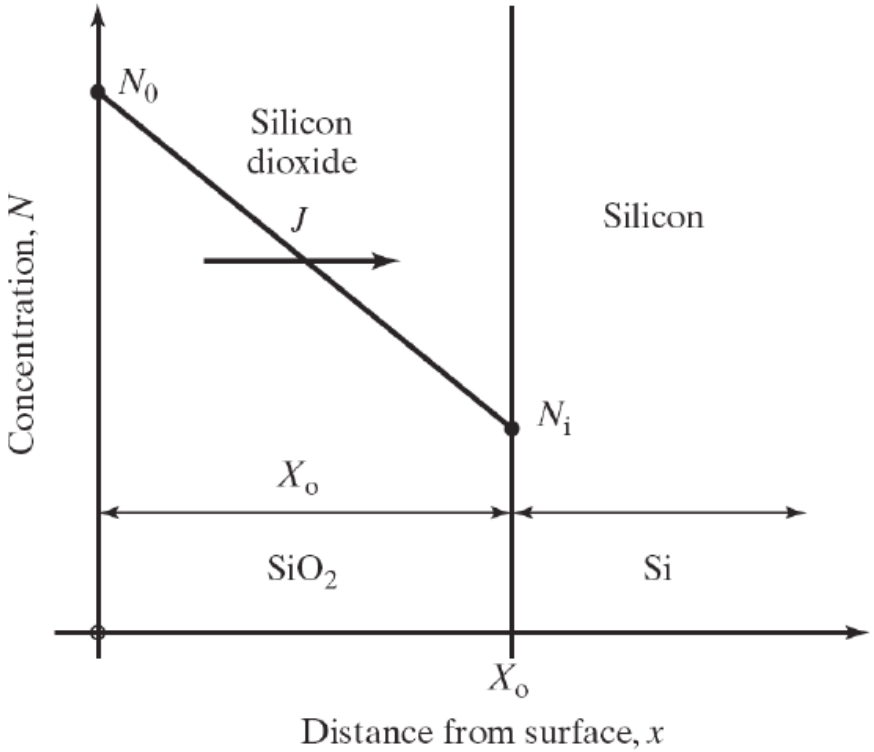


- Diffusion Mechanisms
  - Substitutional
  - Interstitial

FIGURE 4.1

Atomic diffusion in a two-dimensional lattice. (a) Substitutional diffusion, in which the impurity moves among vacancies in the lattice; (b) interstitialcy mechanism, in which the impurity atom replaces a silicon atom in the lattice, and the silicon atom is displaced to a interstitial site; (c) interstitial diffusion, in which impurity atoms do not replace atoms in the crystal lattice.

4. Diffusion Process: Fick's First Law

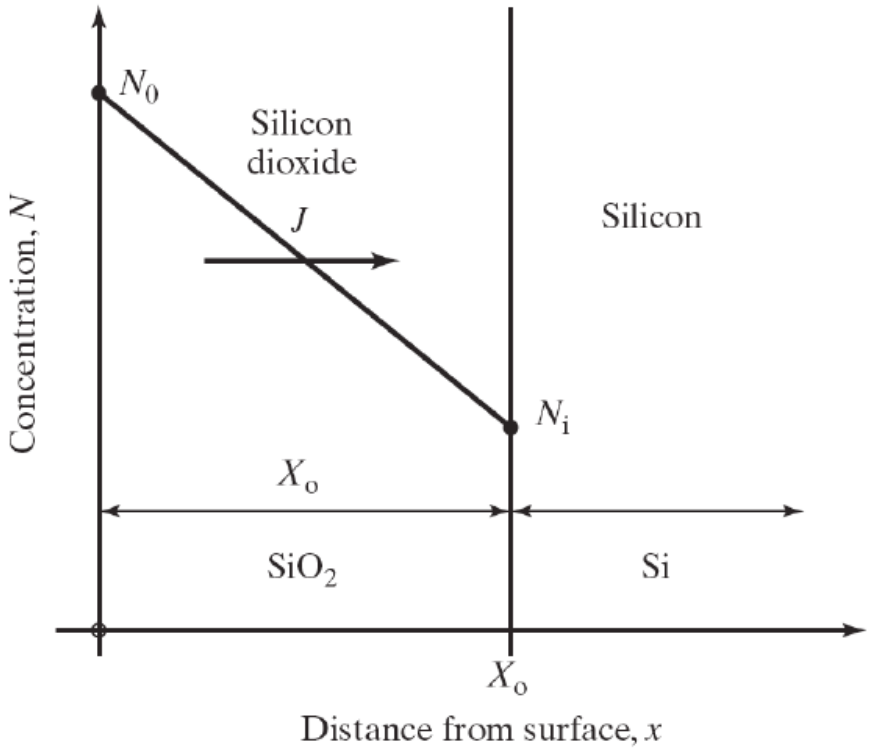


Particle flux J is proportional to the negative of the gradient of the particle concentration

$$J = -D\frac{\partial N}{\partial x}$$

D = diffusion coefficient

4. Diffusion Process: Fick's Second Law



Continuity Equation for Particle Flux :

Rate of increase of concentration is equal to the negative of the divergence of the particle flux

$$\frac{\partial N}{\partial t} = -\frac{\partial J}{\partial x}$$

(in one dimension)

Fick's Second Law of Diffusion :

Combine First Law with Continuity Eqn.

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2}$$

D assumed to be independent of concentration!

4. Diffusion Process: Profile Function 1 = Complementary Error Function

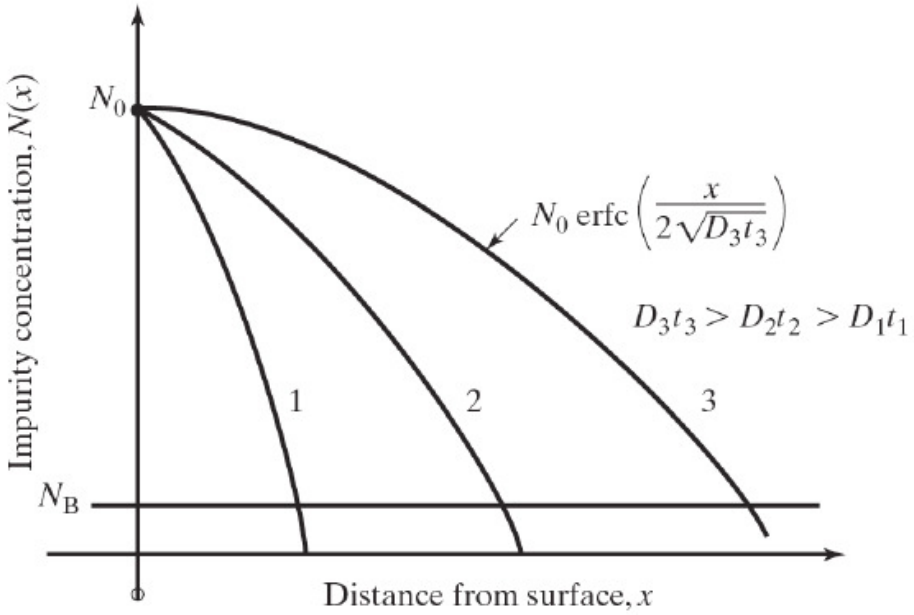


FIGURE 4.2

A constant-source diffusion results in a complementary error function impurity distribution. The surface concentration N_0 remains constant, and the diffusion moves deeper into the silicon wafer as the Dt product increases. Dt can change as a result of increasing diffusion time, increasing diffusion temperature, or a combination of both.

Concentration : $$N(x,t) = N_0 erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

Total Dose : $$Q = \int_0^\infty N(x,t)dt = 2N_0\sqrt{\frac{Dt}{\pi}}$$

N_0 = Surface Concentration

D = Diffusion Coefficient

erfc = Complementary Error Function

$$erfc(z) = 1 - erf(z)$$

$$erf(z) = \frac{2}{\sqrt{\pi}}\int_0^z \exp[-x^2]\,dx$$

4. Diffusion Process: Profile Function 2 = Gaussian Function (for a fixed dose)

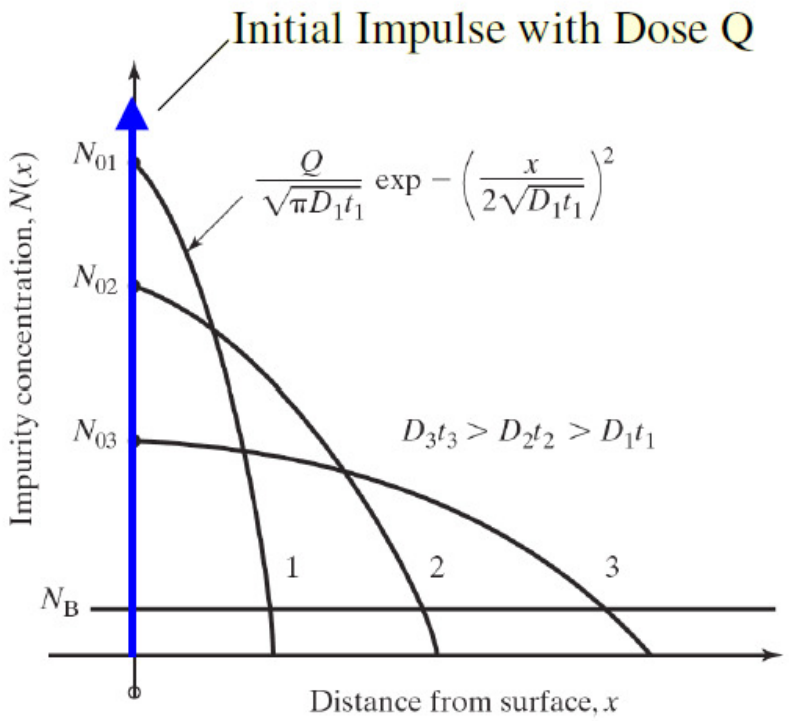


FIGURE 4.3

A Gaussian distribution results from a limited-source diffusion. As the Dt product increases, the diffusion front moves more deeply into the wafer, and the surface concentration decreases. The area (impurity dose) under each of the three curves is the same.

Concentration:

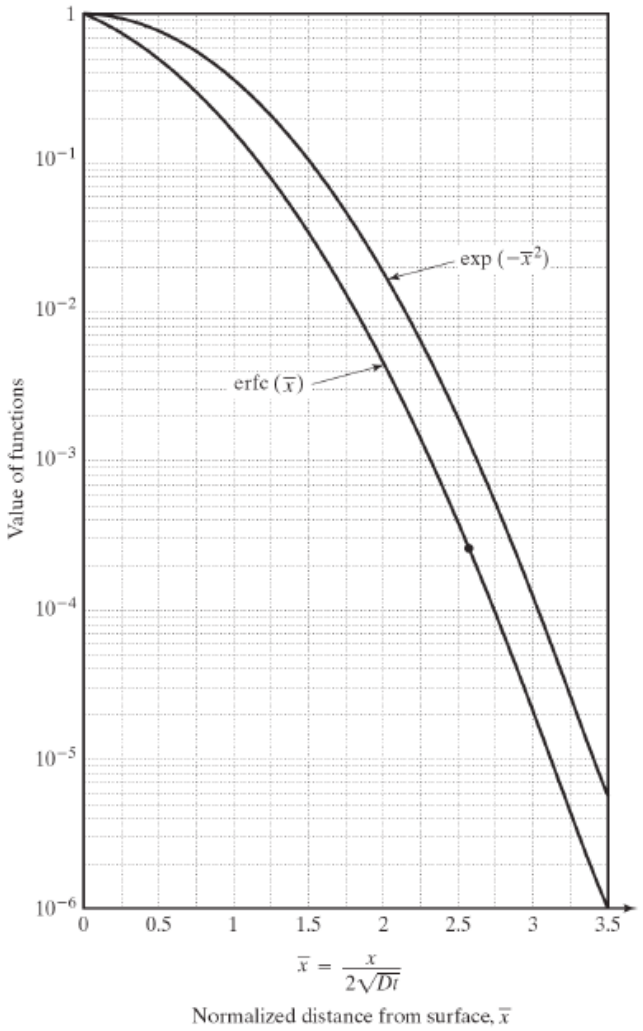
$$N(x,t) = N_0 \exp\left[-\left(\frac{x}{2\sqrt{Dt}}\right)^2\right] = \frac{Q}{\sqrt{\pi Dt}} \exp\left[-\left(\frac{x}{2\sqrt{Dt}}\right)^2\right]$$

N_0 = Surface Concentration $N_0 = \frac{Q}{\sqrt{\pi Dt}}$

D = Diffusion Coefficient

Gaussian Profile

4. Diffusion Process: Comparison



Complementary Error Function and Gaussian Profiles are Similar in Shape

$$erfc(z) = 1 - erf(z)$$

$$erf(z) = \frac{2}{\sqrt{\pi}} \int_0^z \exp\left[-x^2\right] dx$$

FIGURE 4.4

A graph comparing the Gaussian and complementary error function (erfc) profiles. We use this curve to evaluate the erfc and its inverse.

4. Diffusion Process: Diffusion Coefficients

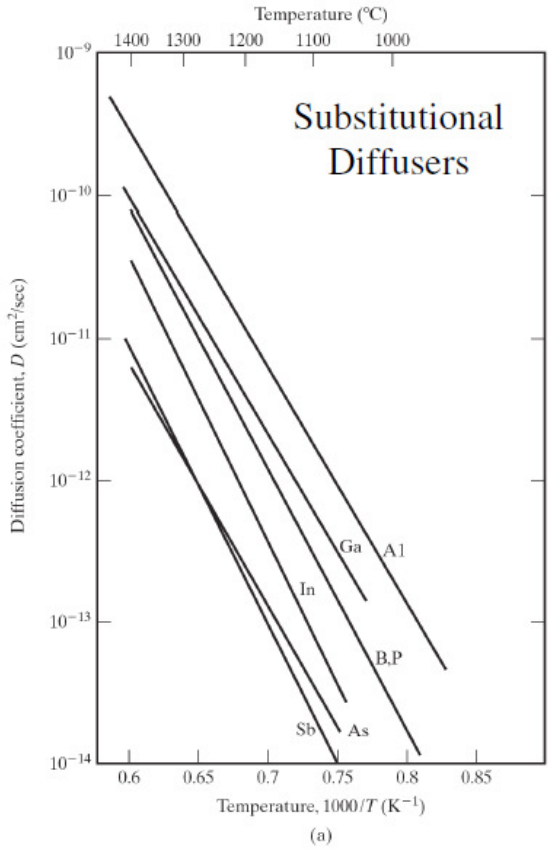
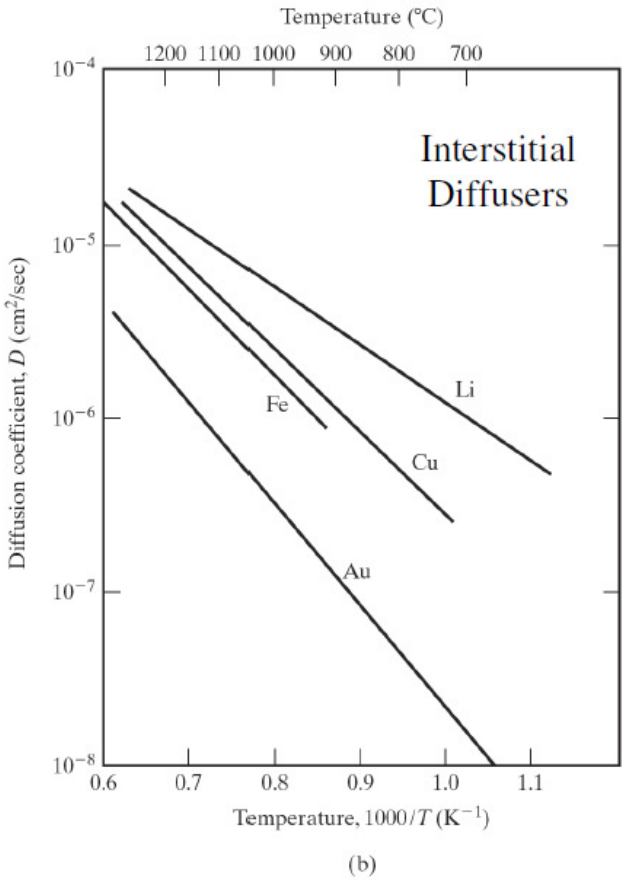


FIGURE 4.5

Diffusion constants in silicon for (a) substitutional diffusers (above) and (b) interstitial diffusers (next page). Copyright John Wiley & Sons, Inc.; reprinted with permission from Ref. [28].



4. Diffusion Process: Diffusion Coefficients and Activation Energy

$$D = D_o \exp\left(-\frac{E_A}{kT}\right)$$ Arrhenius Relationship

E_A = activation energy

k = Boltzmann's constant = 1.38 x10^{-23} J/K

T = absolute temperature

TABLE 4.1 Typical Diffusion Coefficient Values for a Number of Impurities.

Element	D_o(cm^2/sec)	E_A(eV)
B	10.5	3.69
Al	8.00	3.47
Ga	3.60	3.51
In	16.5	3.90
P	10.5	3.69
As	0.32	3.56
Sb	5.60	3.95

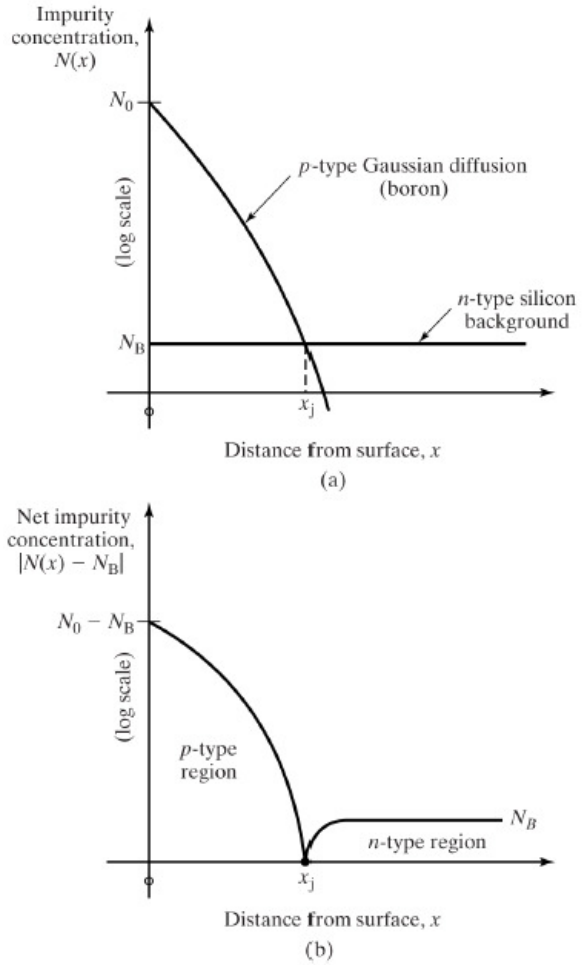
Example 4.1

Calculate the diffusion coefficient for boron at 1100 °C.

Solution: From Table 4.1, $D_o = 10.5$ cm^2/sec and $E_A = 3.69$ eV. $T = 1373$ K.

$$D = 10.5 \exp - \frac{3.69}{(8.614 \times 10^{-5})(1373)} = 2.96 \times 10^{-13} \text{cm}^2/\text{sec}.$$

4. Diffusion Process: P-N Junction (example)



x_j = Metallurgical Junction Depth

P - n junction occurs at the point x_j where the net impurity concentration is zero

(i. e. p - type doping cancels out n - type doping)

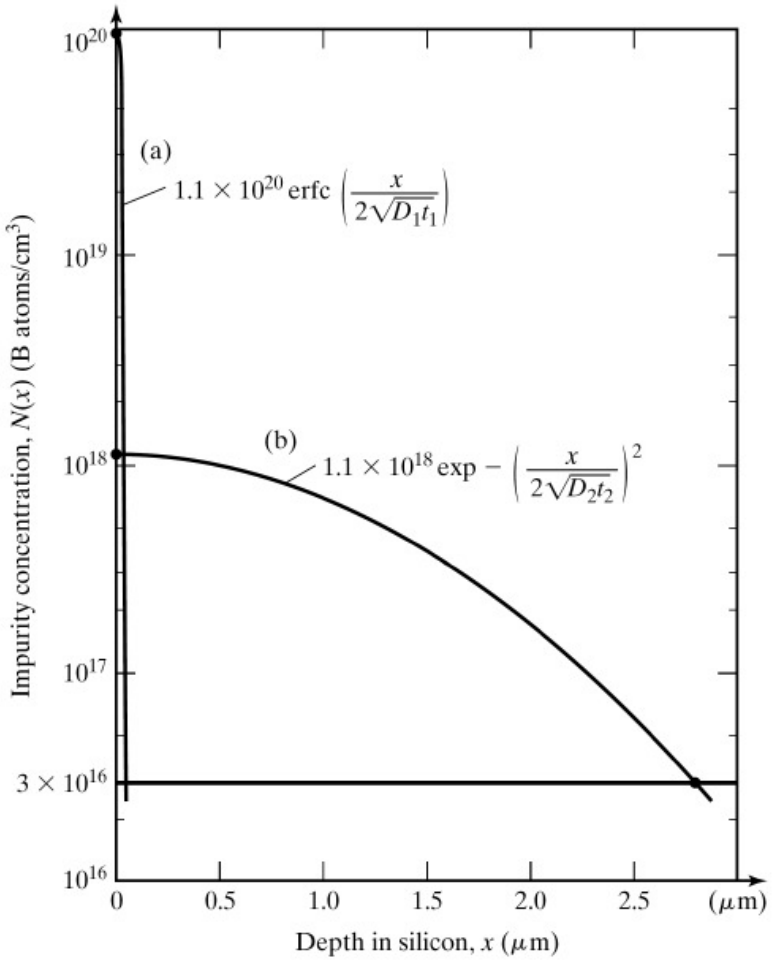
Gaussian Profile : $x_j = 2\sqrt{Dt \ln\left(\frac{N_0}{N_B}\right)}$

Error Function profile : $x_j = 2\sqrt{Dt}\ \mathrm{erfc}^{-1}\left(\frac{N_0}{N_B}\right)$

FIGURE 4.7

Formation of a *pn* junction by diffusion. (a) An example of a *p*-type Gaussian diffusion into a uniformly doped *n*-type wafer; (b) net impurity concentration in the wafer. The metallurgical junction occurs at the point $x = x_j$ where the net concentration is zero. The material is converted to *p*-type to the left of x_j and remains *n*-type to the right of x_j.

4. Diffusion Process: Two-Step Diffusion

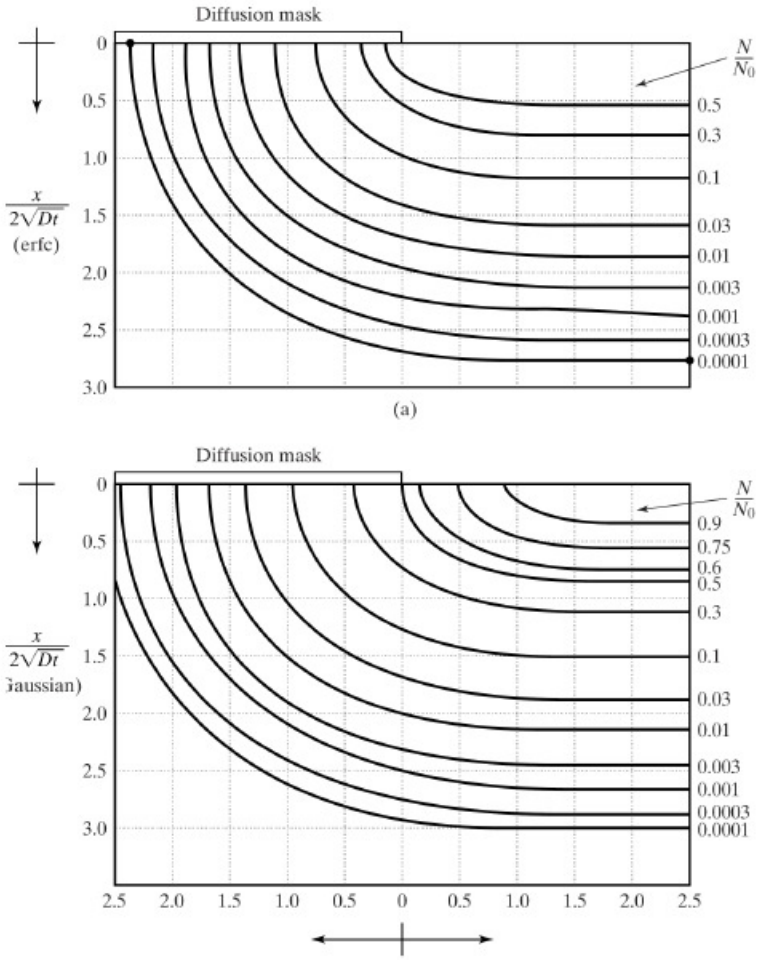


- Short constant source diffusion used to establish dose Q ("Predep" step)
- Longer limited source diffusion drives profile in to desired depth ("drive in" step)
- Final profile is Gaussian

FIGURE 4.9

Calculated boron impurity profiles for Example 4.2. (a) Following the predeposition step at 900°C for 15 min; (b) following a subsequent 5-hr drive-in step at 1,100°C. The final junction depth is 2.77 μm with a surface concentration of 1.1×10^{18}/cm^3. The initial profile approximates an impulse.

4. Diffusion Process: Masking



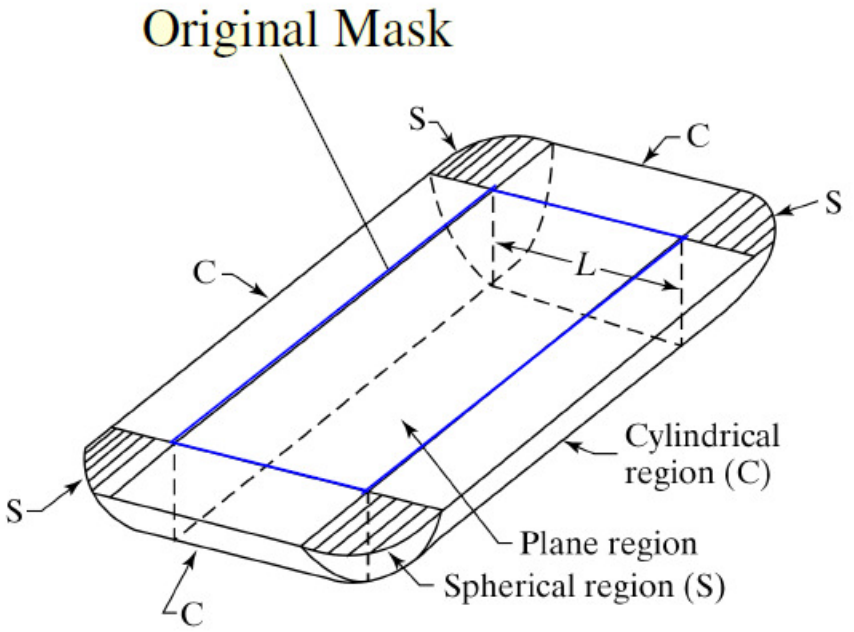
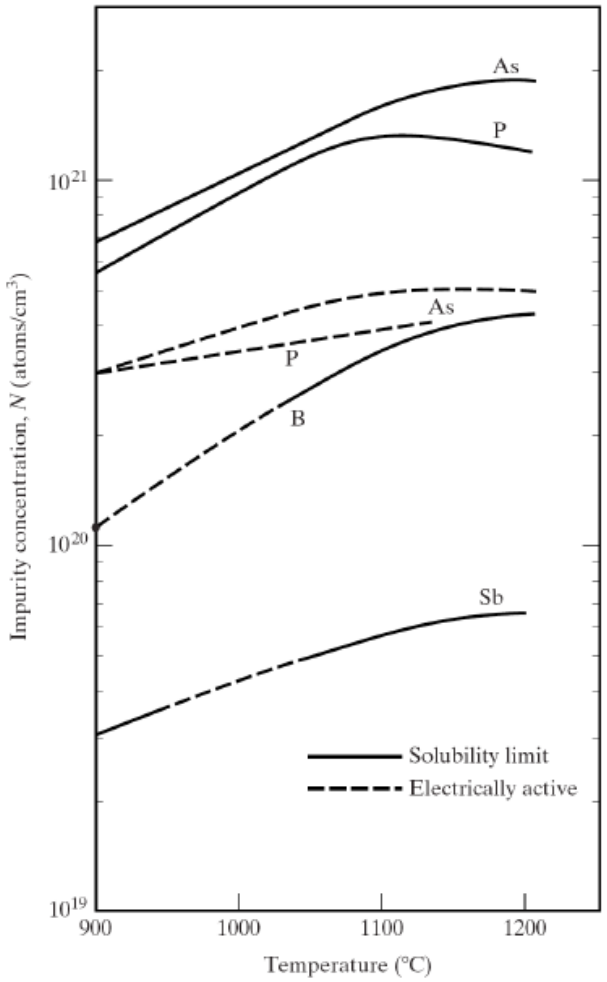


FIGURE 4.10

Normalized two-dimensional complementary error function and Gaussian diffusions near the edge of a window in the barrier layer. Copyright 1965 by International Business Machines Corporation; reprinted with permission from Ref. [4].

4. Diffusion Process: Limit of Diffusion = Solid Solubility Limit



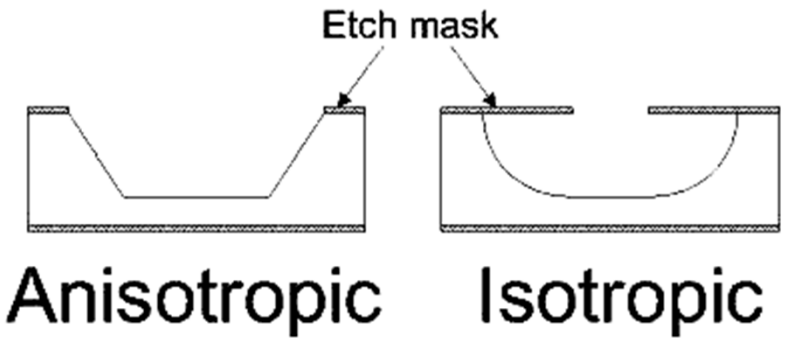
- There is a limit to the amount of a given impurity that can be "dissolved" in silicon (the Solid Solubility Limit)
- At high concentrations, all of the impurities introduced into silicon will not be electrically active

FIGURE 4.6

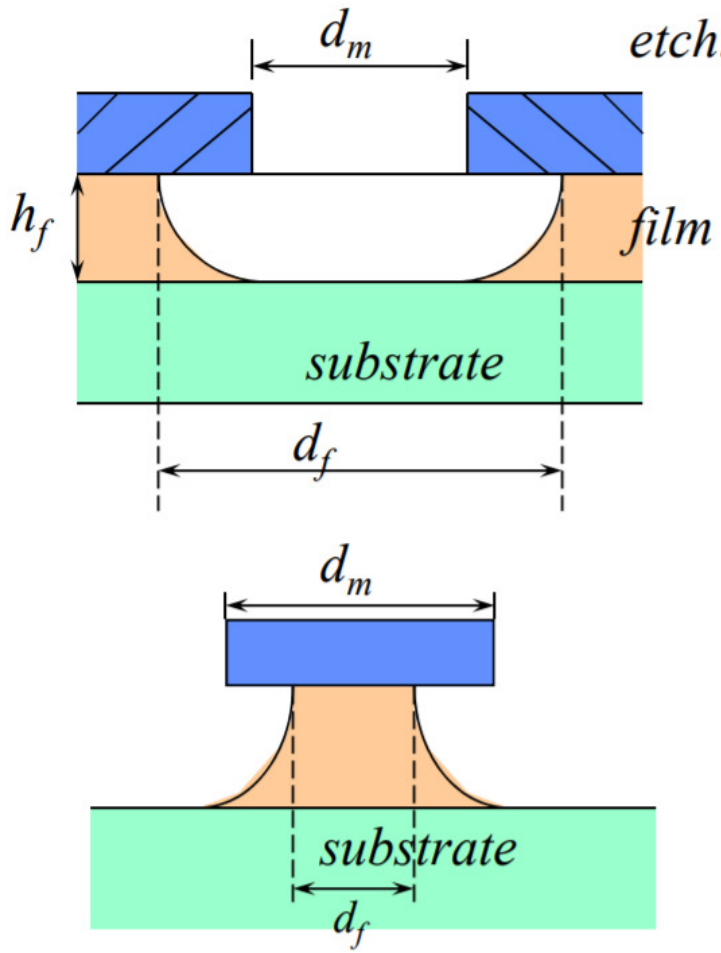
The solid-solubility and electrically active impurity-concentration limits in silicon for antimony, arsenic, boron, and phosphorus. Reprinted with permission from Ref. [29]. This paper was originally presented at the 1977 Spring Meeting of The Electrochemical Society, Inc., held in Philadelphia, Pennsylvania.

5. Etching: Figure of Merit

- Etch rate
- Etch rate uniformity
- Selectivity
- Anisotropy



5. Etching: Wet etching (Isotropic)

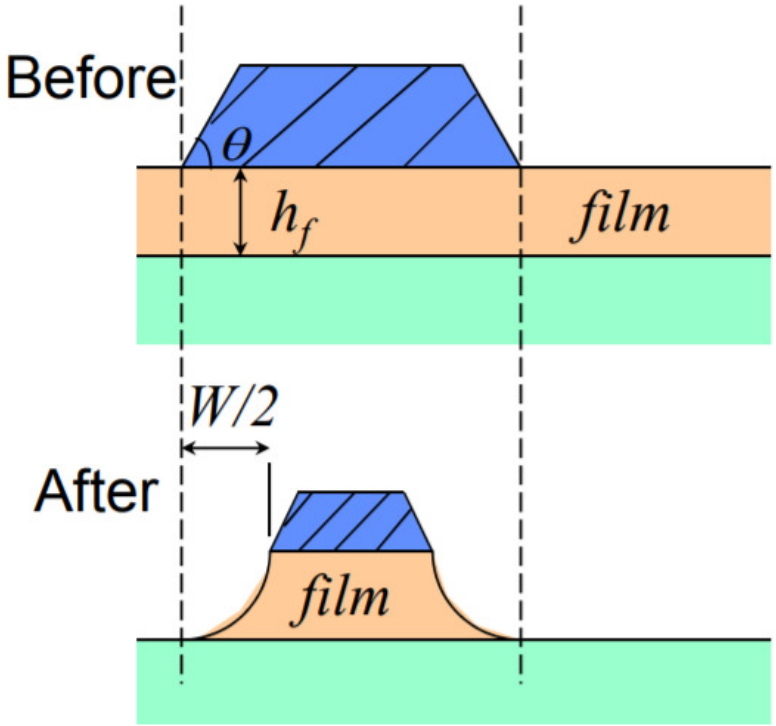


$$Bias\ B \equiv d_f - d_m$$

$$B\ can\ be > 0\ or < 0.$$

5. Etching: Wet etching selectivity

State-of-problem:
Mask material can be eroded during film etching.
Top of film will be smaller than original mask size by an amount W/2.



Let $v_{m\perp}$, $v_{m//}$ be the vertical and lateral etching rates of the mask.

Let v_f be the vertical etching rate of the film.

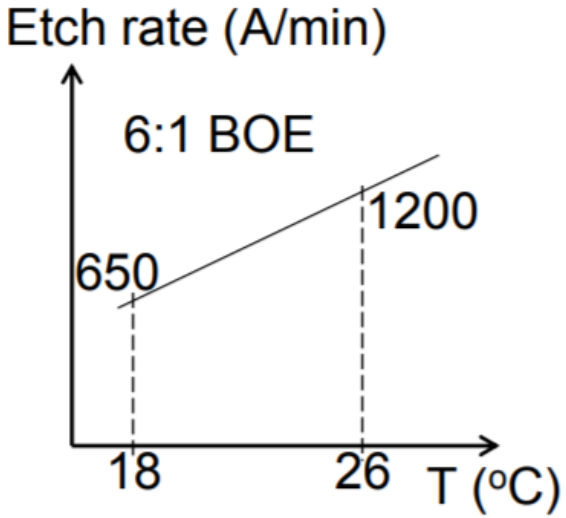
(lateral film etch rate is ignored In this example for simplicity)

5. Etching: Wet Etching of Insulator (example: SiO_2)

Silicon Dioxide

To etch SiO_2 film on Si, use

$HF + H_2O$



$$SiO_2 + 6HF \rightarrow H_2 + SiF_6 + 2H_2O$$

Note: HF is usually buffered with NH_4F to maintain $[H^+]$ at a constant level (for constant etch rate)

$$NH_4F \rightarrow NH_3 + HF$$

5. Etching: Wet Etching of Metal (example: Aluminum)

Aluminum

To etch Al film on Si or SiO_2, use

$$H_3PO_4 + CH_3COOH + HNO_3 + H_2O$$

(phosphoric acid) *(acetic acid)* *(nitric acid)*

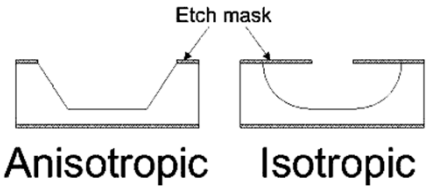
(~30°C)

$$6H^+ + 2Al \rightarrow 3H_2 + 2Al^{3+}$$

(Al^{3+} is water-soluble)

5. Etching: Wet Etching of Semiconductor (example: Silicon)

Silicon



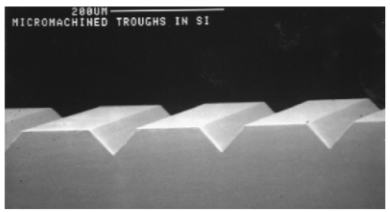
(i) Isotropic etching

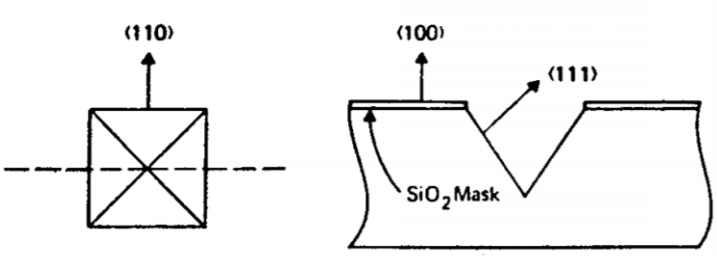
Use HF + HNO_3 + H_2O

$3Si + 4HNO_3 \rightarrow 3SiO_2 + 4NO + 2H_2O$

$3SiO_2 + 18HF \rightarrow 3H_2SiF_6 + 6H_2O$

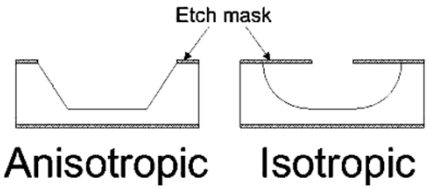
(ii) **Anisotropic etching (e.g. KOH, EDP)**





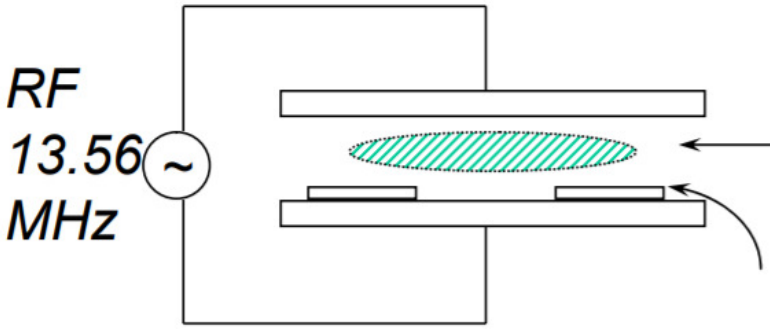
5. Etching: Wet Etching Issues

- Lack of anisotropy
- Poor process control
- Excessive particulate contamination



=> Wet etching used for **noncritical** feature sizes

5. Etching: Dry Etching (RIE)

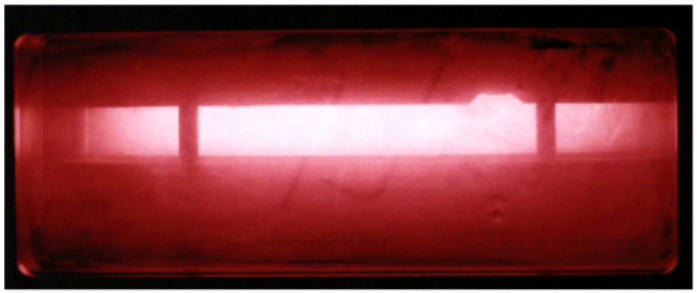


Parallel-Plate Reactor

Sputtering

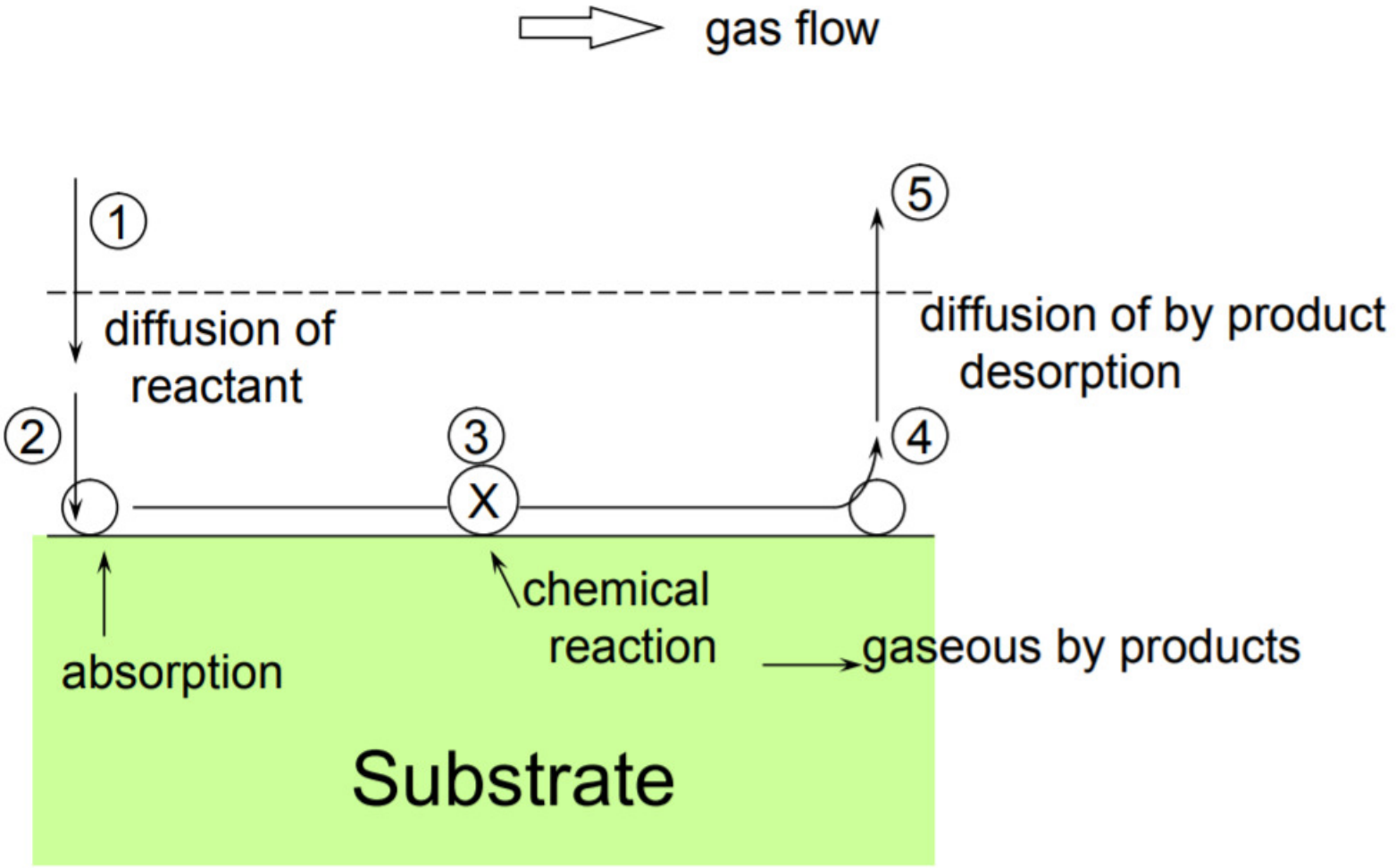
Plasma generates (1) Ions

(2) Activated neutrals



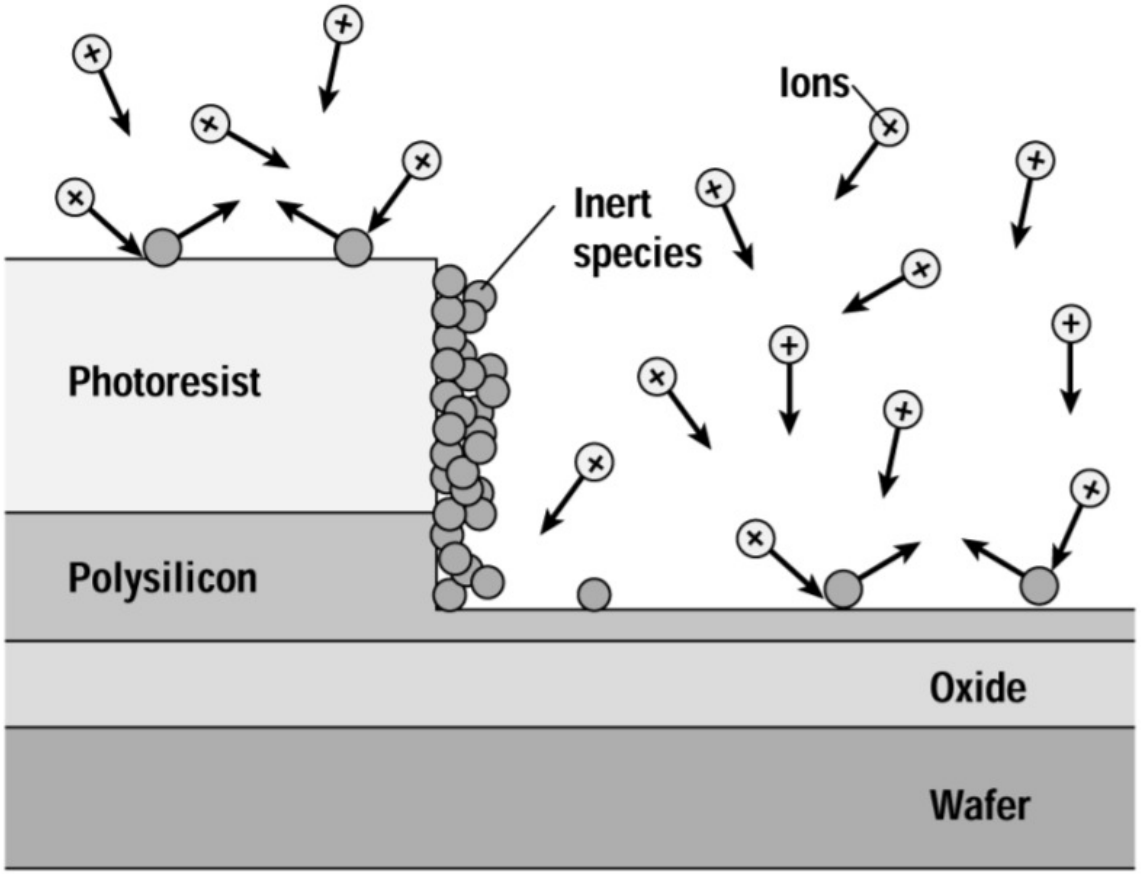
Enhance chemical reaction

5. Etching: Dry Etching (RIE) Sequence



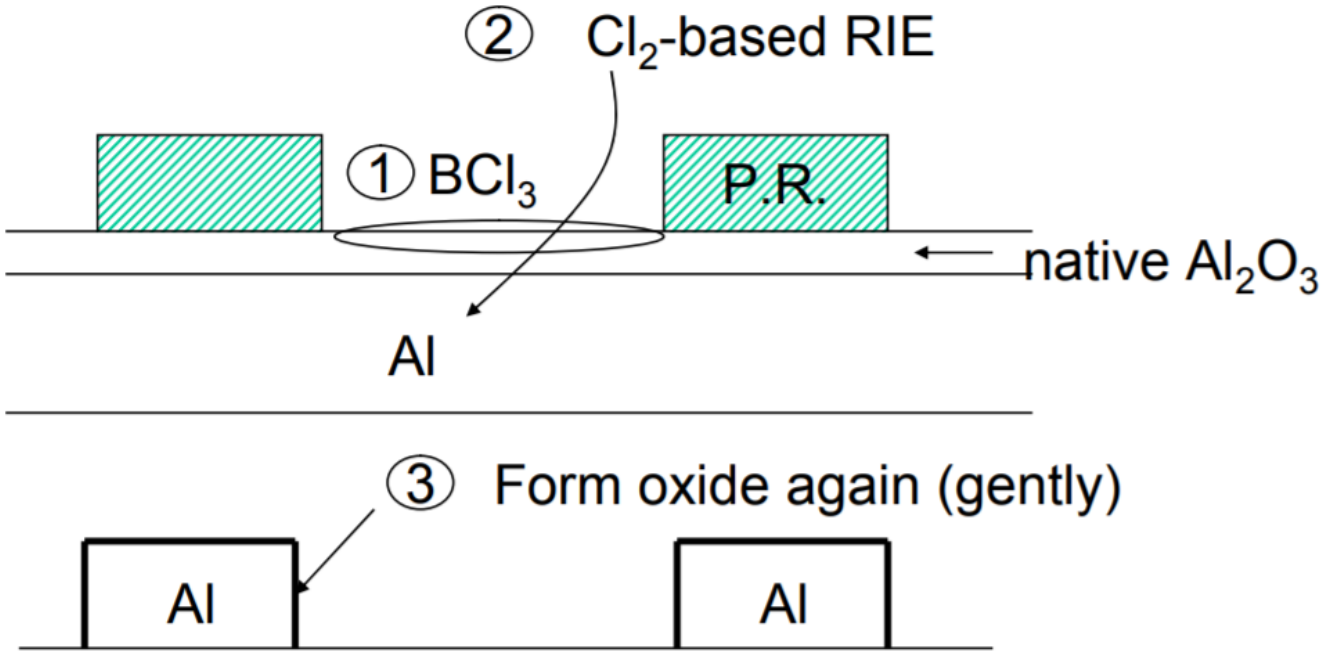
5. Etching: Dry Etching (RIE) Issues

REMOVAL of surface film and **DEPOSITION** of plasma reaction products can occur simultaneously

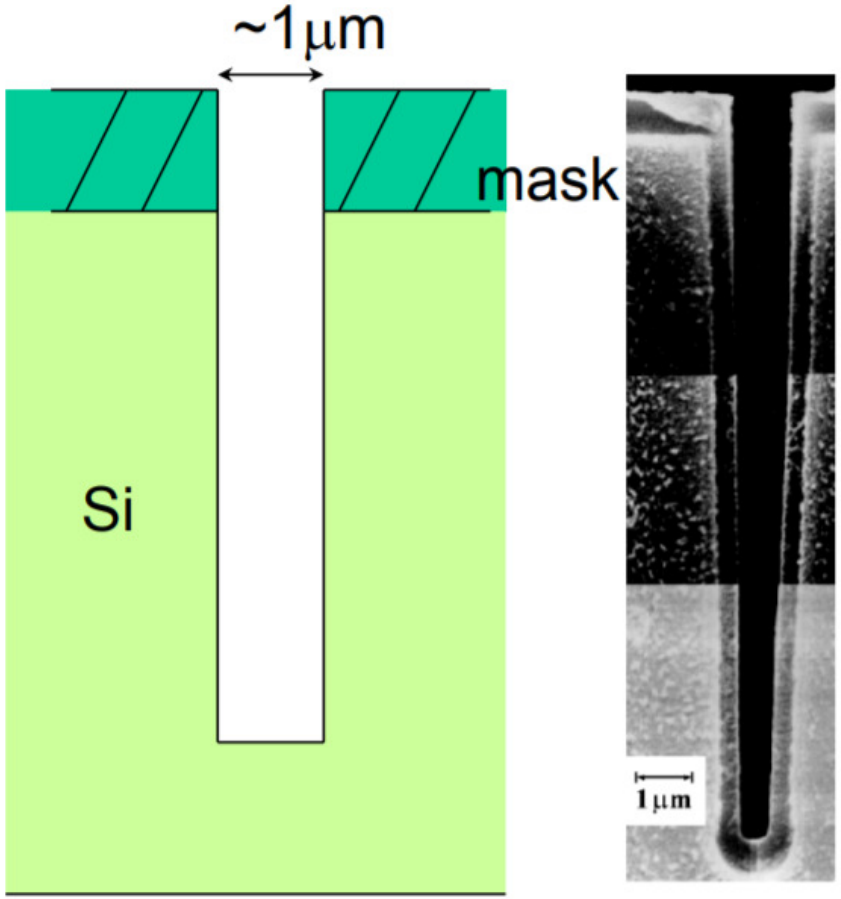


5. Etching: RIE Example (Aluminum)

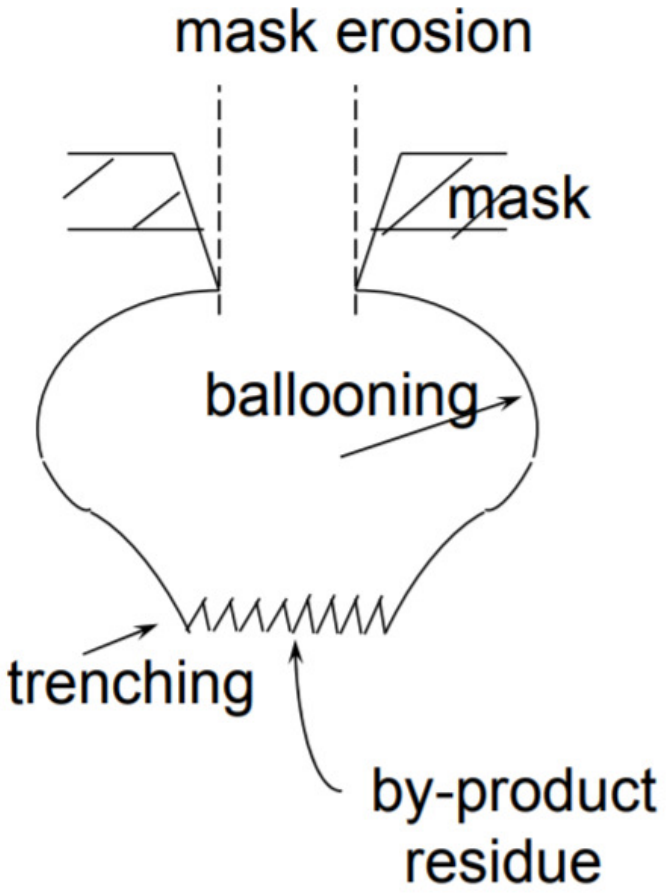
* It is a three-step sequence :
1) Remove native oxide with BCl_3
2) Etch Al with Cl-based plasma
3) Protect fresh Al surface with thin oxidation



5. Etching: RIE Example (Deep Trench)



"ideal"



"problems"

6. Film Deposition: CVD (Chemical Vapor Deposition)

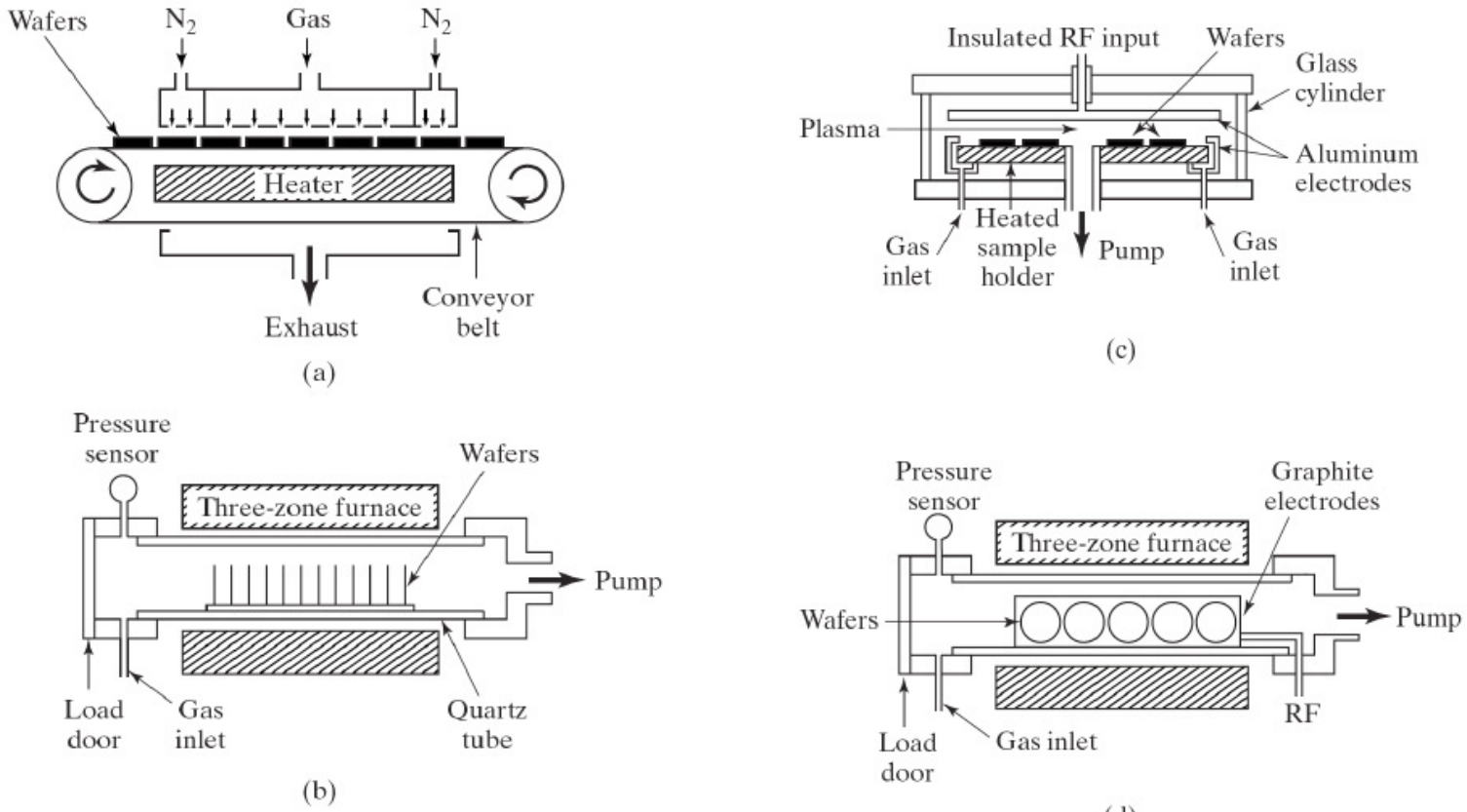
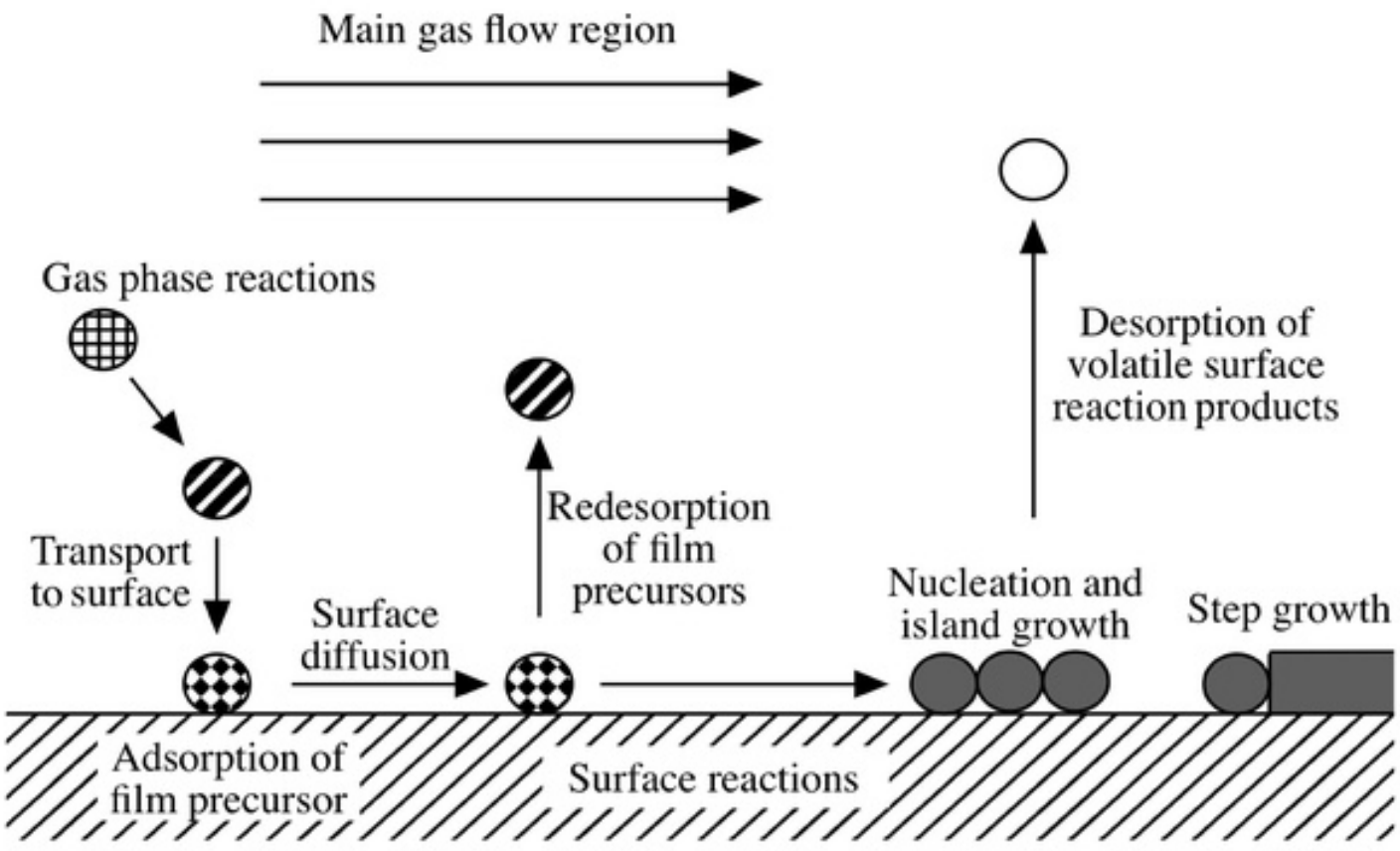


Figure 6.8
Four types of CVD systems. (a) Atmospheric-pressure reactor (b) hot-wall low-pressure (LPCVD) system in a three-zone furnace (c) parallel-plate plasma-enhanced system (d) photo-enhanced (PECVD) system using a three-zone furnace. Copyright 1983 Bell Telephone Laboratories, Inc. Reprinted with permission from Ref. [2].

6. Film Deposition: CVD Process



6. Film Deposition: CVD Example: Poly-Si

- Low Pressure Chemical Vapor Deposition (LPCVD)
  - 25-150 Pa

- Thermal Decomposition of Silane
  - 100% Silane
  - 20-30% Silane in Nitrogen

$$SiH_4 \xrightarrow{600^o C} Si + 2H_2$$

  - 100-200 Å/min at 600-650° C

6. Film Deposition: CVD Example: Metal

Tungsten - Thermal, Plasma or Optical Assisted Decomposition of WF_6

$$WF_6 \rightarrow W + 3F_2$$

Tungsten - Reduction of WF_6 with Hydrogen

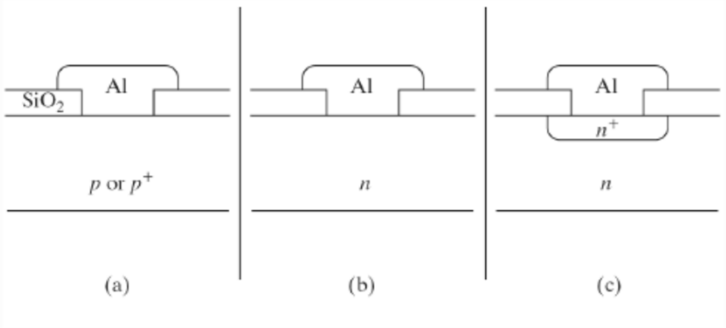
$$WF_6 + 3H_2 \rightarrow W + 6HF$$

Mo, Ta and Ti - LPCVD Reaction with Hydrogen

$$2MCl_5 + 5H_2 \rightarrow 2M + 10HCl$$

Copper is Deposited by "Standard" Plating Techniques

6. Film Deposition: CVD Example: Metal: Contact



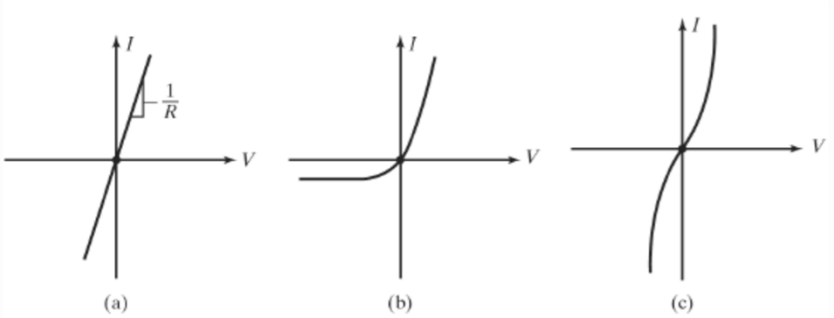


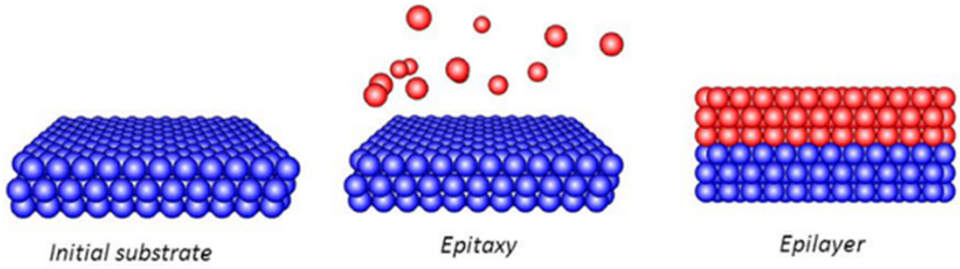
Figure 7.2

Figure 7.3

- Aluminum to p-type silicon forms an ohmic contact similar to Fig. 7.2(a) [Remember Al is p-type dopant]
- Aluminum to n-type silicon can form a rectifying contact (Schottky barrier diode) similar to Fig. 7.3(b)
- Aluminum to n+ silicon yields a contact similar to Fig. 7.3c

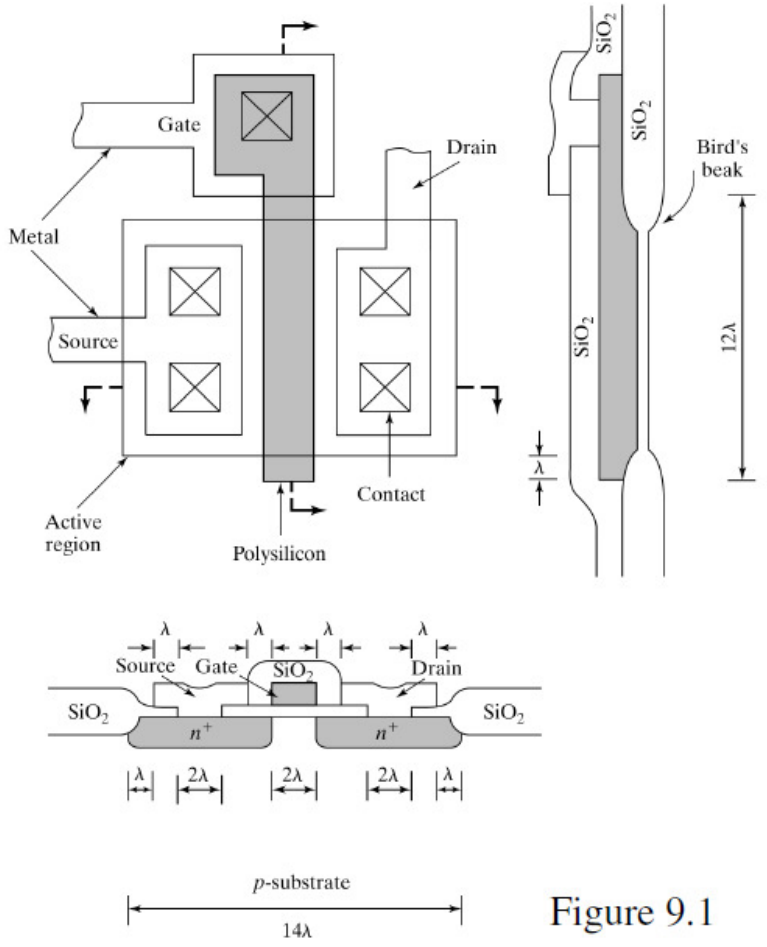
6. Film Deposition: Epitaxy (direct deposition without precursors)

- Vapor Phase Epitaxy
- Liquid Phase Epitaxy
  - Compound Semiconductors
- Molecular Beam Epitaxy
  - Compound Semiconductors
- III-V Compound Semiconductors
  - GaAs, InP, GaInAs, InAs …



Part 2. Appendix:
MOSFET Process and Issues

MOSFET Structure and Model



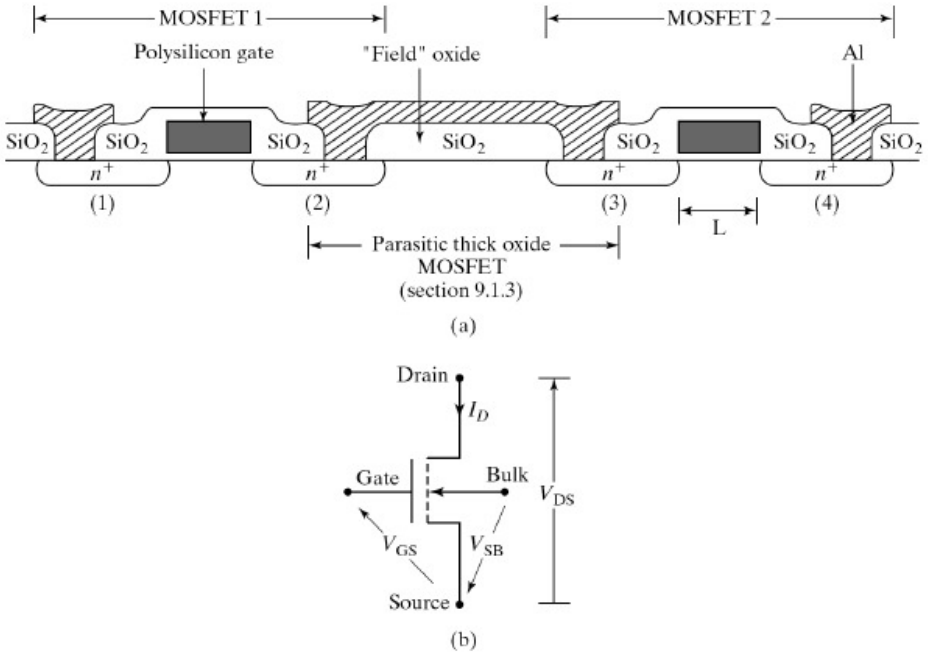


Figure 9.1

$$I_D = K_n'\left(\frac{W}{L}\right)\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS} \qquad K_n' = \mu_n C_O = \mu_n \frac{\varepsilon_{OX}}{X_O}$$

$$V_{GS} > V_{TN} \qquad V_{TN} = \text{threshold voltage}$$

Threshold Voltage and Substrate Doping Density

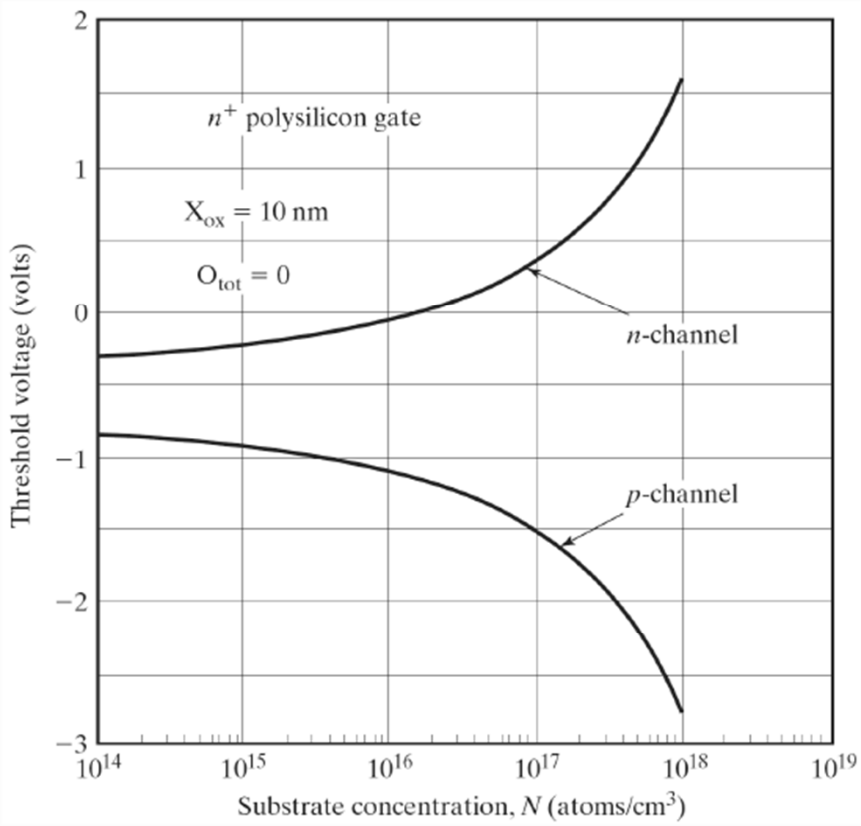


Figure 9.2
Threshold voltage vs. substate doping

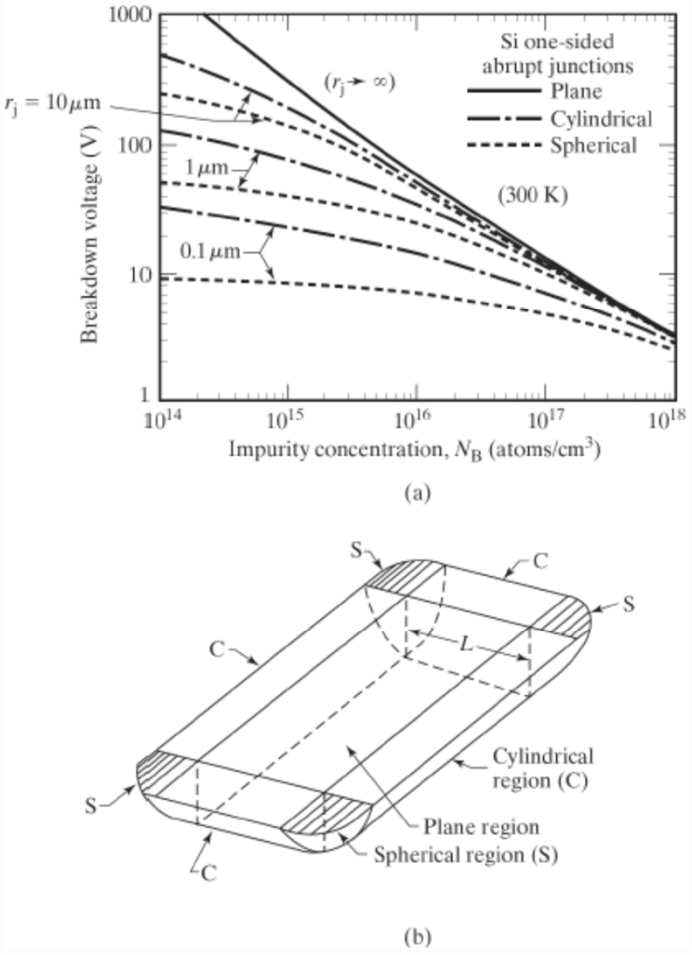
$$V_{TN} = \Phi_M - \chi - \frac{E_G}{2q} + |\phi_F| + \frac{\sqrt{2K_S\varepsilon_o qN_B(2|\phi_F| + V_{SB})}}{C_O} - \frac{Q_{tot}}{C_O}$$

$$V_{TP} = \Phi_M - \chi - \frac{E_G}{2q} - |\phi_F| - \frac{\sqrt{2K_S\varepsilon_o qN_B(2|\phi_F| + V_{SB})}}{C_O} - \frac{Q_{tot}}{C_O}$$

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_B}{n_i}\right)$$

Φ_M = metal - semiconductor work function
χ = electron affinity
$\Phi_M - \chi = -0.11$ V for aluminum gates
$\Phi_M - \chi = -0$ V for an n^+ polysilicon gate
$\Phi_M - \chi = +1.12$ V (E_G) for a p^+ polysilicon gate
Q_{tot} = total oxide charge

Substrate Doping and Junction Breakdown



- Substrate doping must be selected to support required drain-substrate voltage
- Light doping increases breakdown voltage
- Cylindrical and spherical curvatures reduce the breakdown voltage

FIGURE 9.3

(a) Abrupt *pn* junction breakdown voltage versus impurity concentration on the lightly doped side of the side of the junction for both cylindrical and spherical structures. r_j is the radius of curvature. (b) Formation of cylindrical and spherical regions by diffusion through a rectangular window. Copyright 1985, John Wiley & Sons, Inc. Reprinted with permission from Ref. [5].

Substrate Doping and Depletion Layer Widths

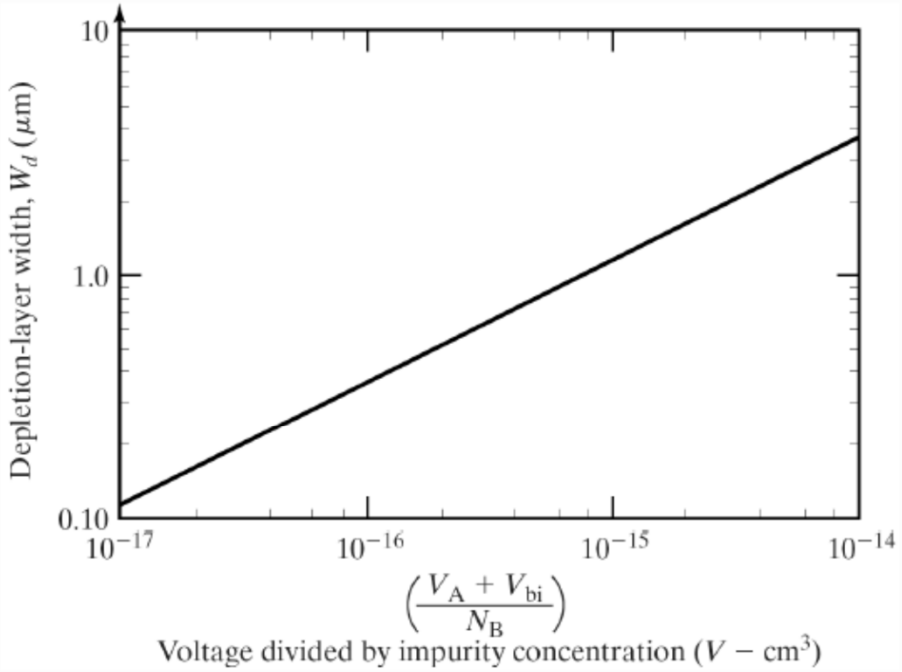
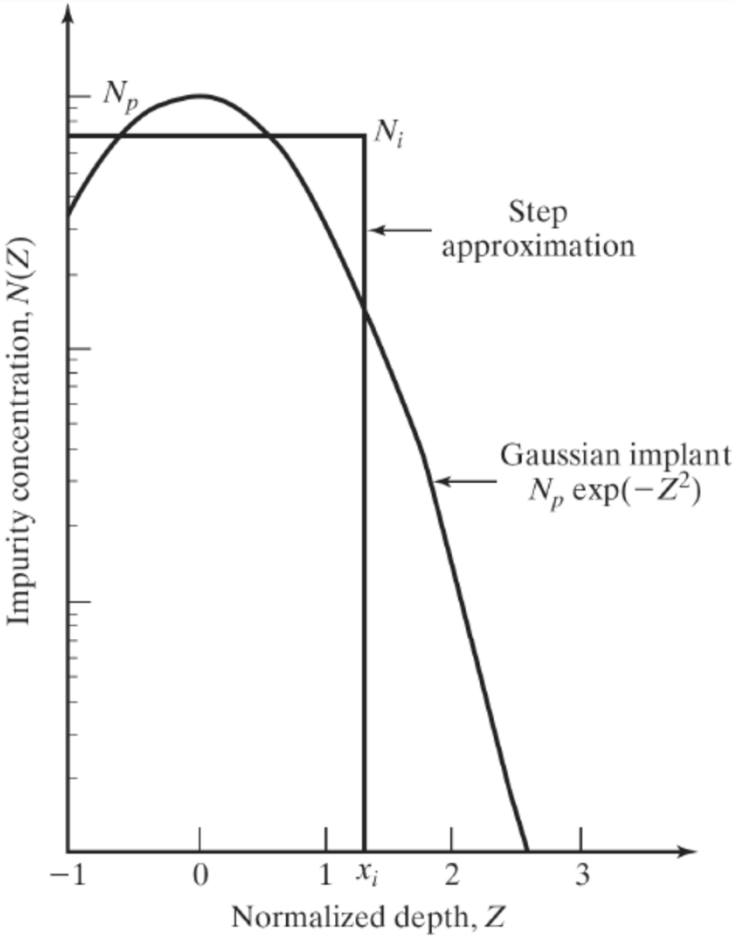


Figure 9.4
Depletion-layer width of a one-sided step junction as a function of doping and applied voltage

- NMOS transistors are "self isolating"
- However, depletion layer widths limit minimum device separation
- Light doping reduces junction capacitances

Threshold Voltage Adjustment Implantation



- Threshold adjustment implants provide additional variable that allows threshold voltage to be designed independently from substrate doping

$$\Delta V_{TN} = \left(\frac{qQ_i}{C_O}\right)\left(1 - \frac{x_i}{2x_d}\right) \quad \text{for} \quad x_i << x_d$$

$$x_d = \sqrt{\frac{qN_B}{4K_S\varepsilon_o|\phi_F|}}$$

Figure 9.5
Step approximation to a Gaussian impurity profile used to estimate the threshold-voltage shift achieved using ion implantation

Threshold Voltage Adjustment Implantation to get depletion mode operation

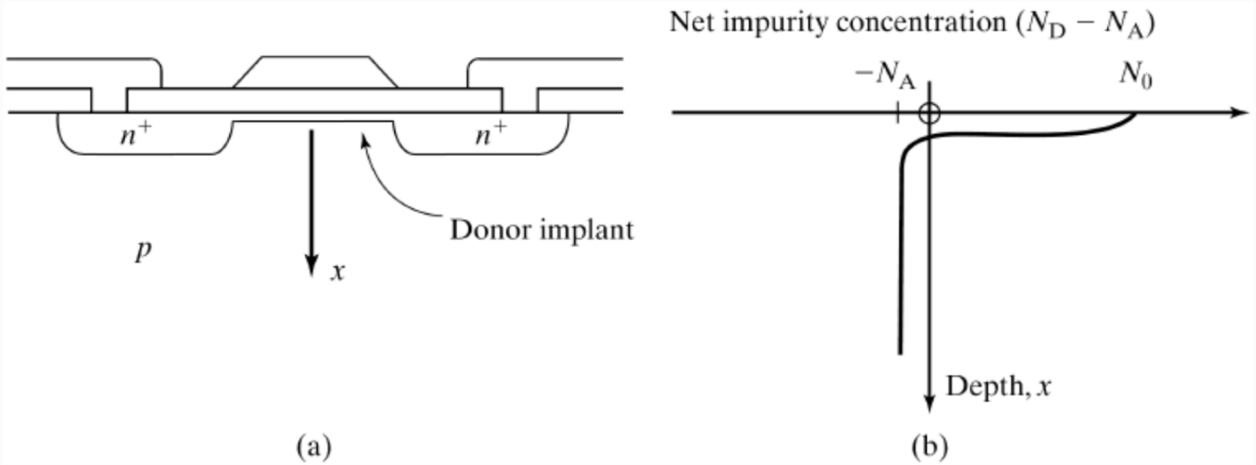


Figure 9.6

- Threshold adjustment implant can create built-in channel connecting source and drain thereby creating NMOS depletion-mode device ($V_{TN} \leq 0$)
- Depletion-mode devices significantly enhance the performance of NMOS logic circuits and analog circuits

Shallow Trench Isolation

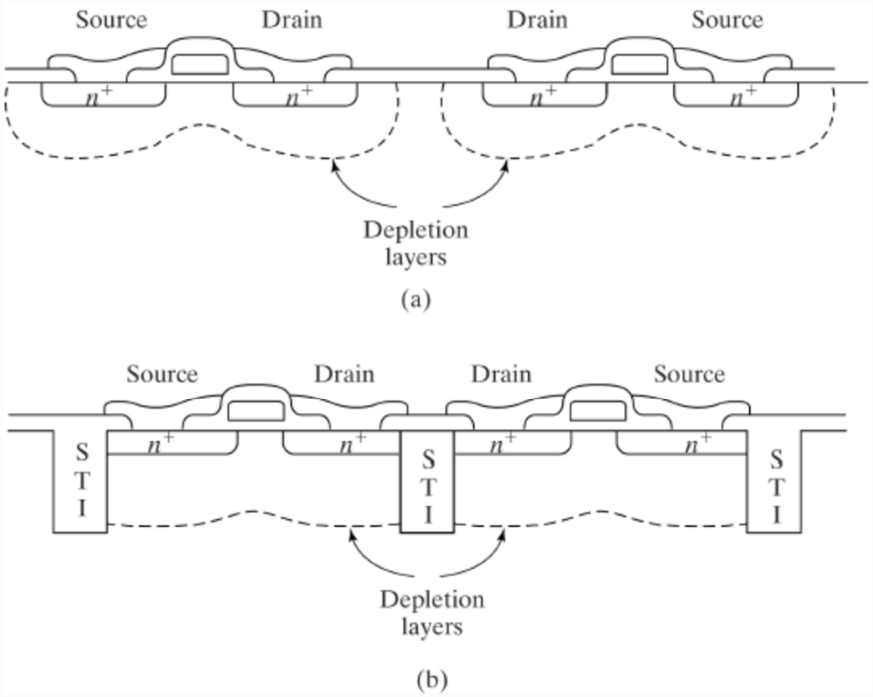


Figure 9.7
Isolation Techniques (a) Intrinsic (b) Shallow trench

- Depletion layers from adjacent devices must not merge
- Shallow trench isolation reduces separation required between devices

Lightly Doped Drains (LDD)

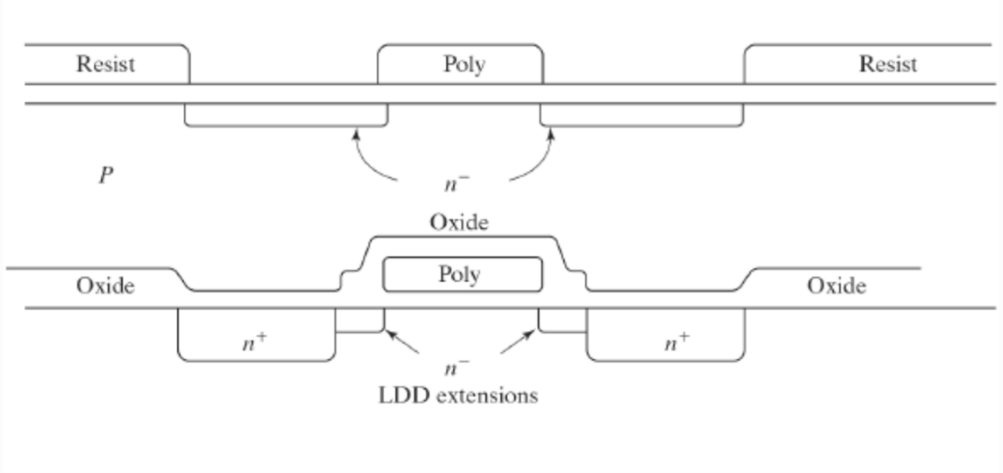


Figure 9.8
Self-aligned polysilicon-gate transistor with lightly doped source/drain regions

- Heavy doping in drain near edge of channel reduces breakdown voltage of the device and reduces reliability
- LDD structure reduce drain doping at edge of channel

Mask Alignment Errors

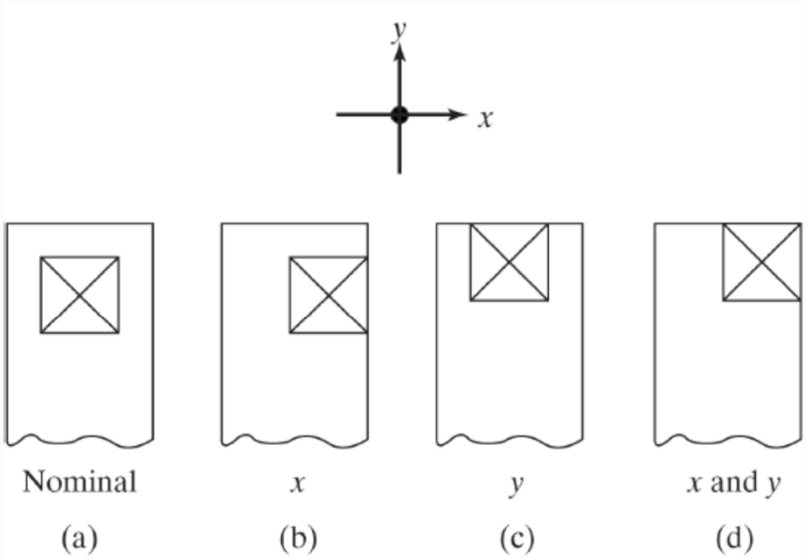
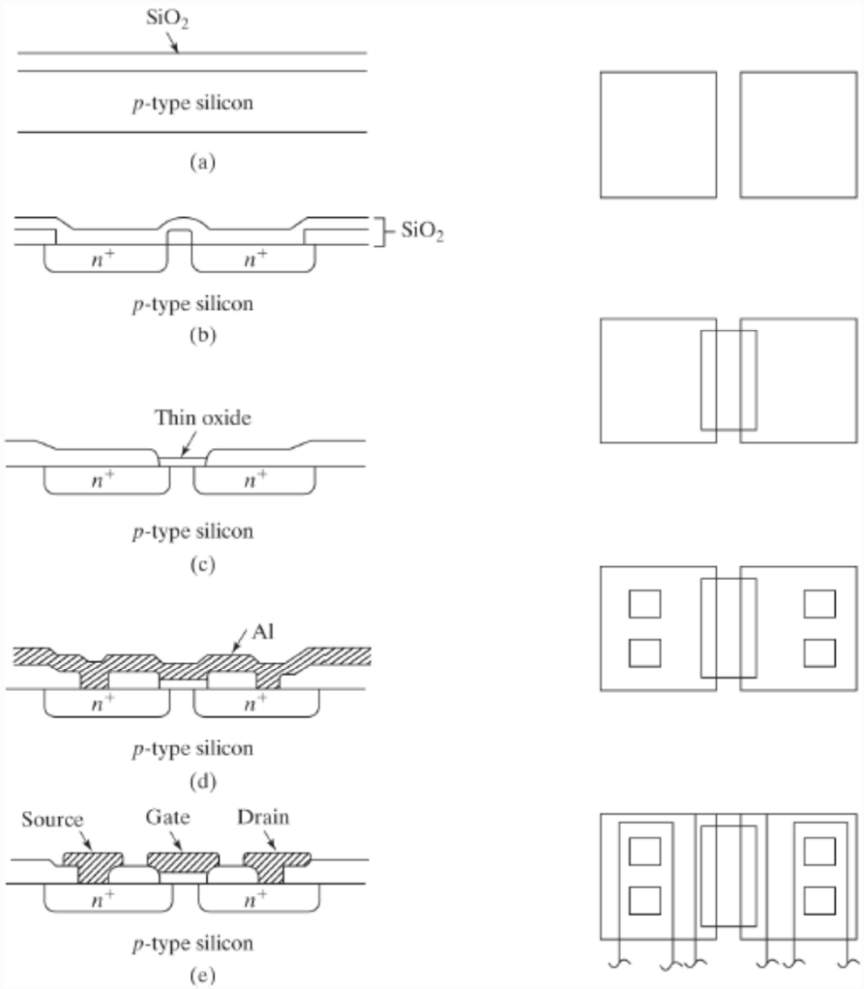


Figure 9.9

- Levels must overlap by at least one alignment tolerance to ensure coverage and proper device operation
- Figure shows various possible misalignments between two levels

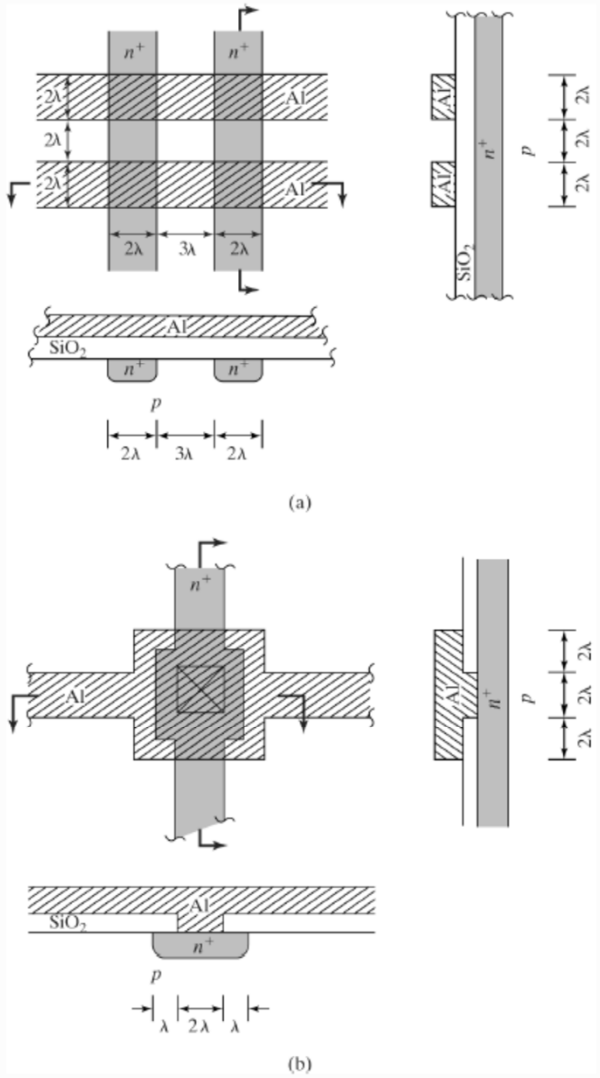
Mask Sequence



- One Alignment Sequence
  1. Source/Drain - first mask level
  2. Thin oxide - align to first level
  3. Contacts - align to first level
  4. Metal - align to level 2

Figure 9.10

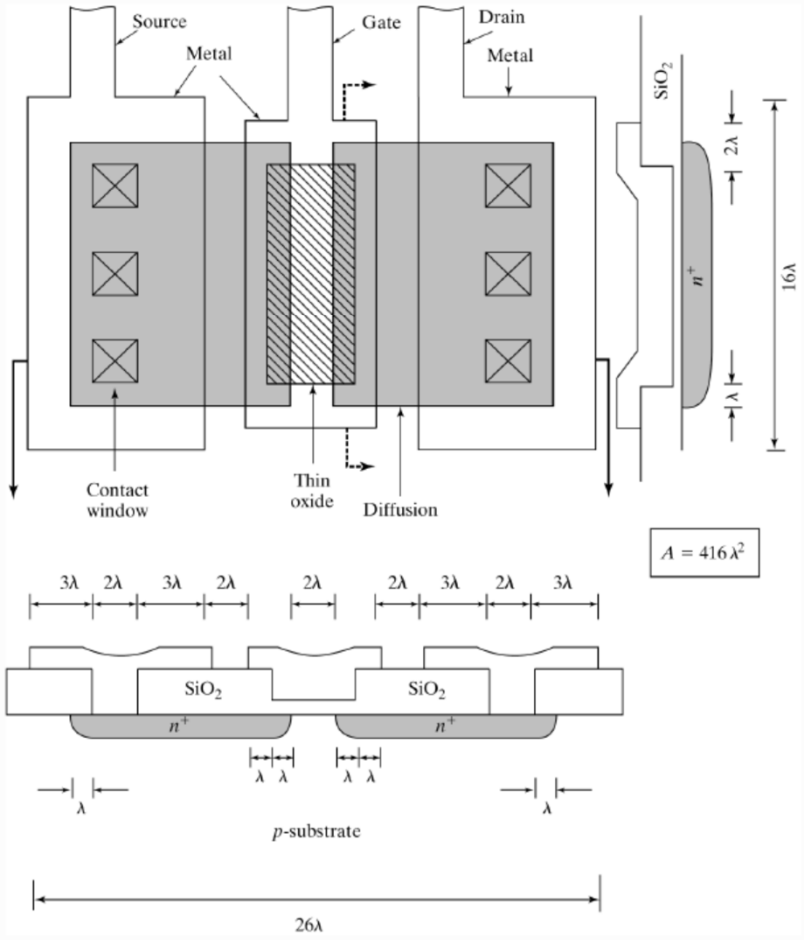
Typical Design (Layout) Rule



- Design rules for previous alignment sequence
- Minimum Feature Size F = 2λ
- Alignment Tolerance T = λ

Figure 9.11

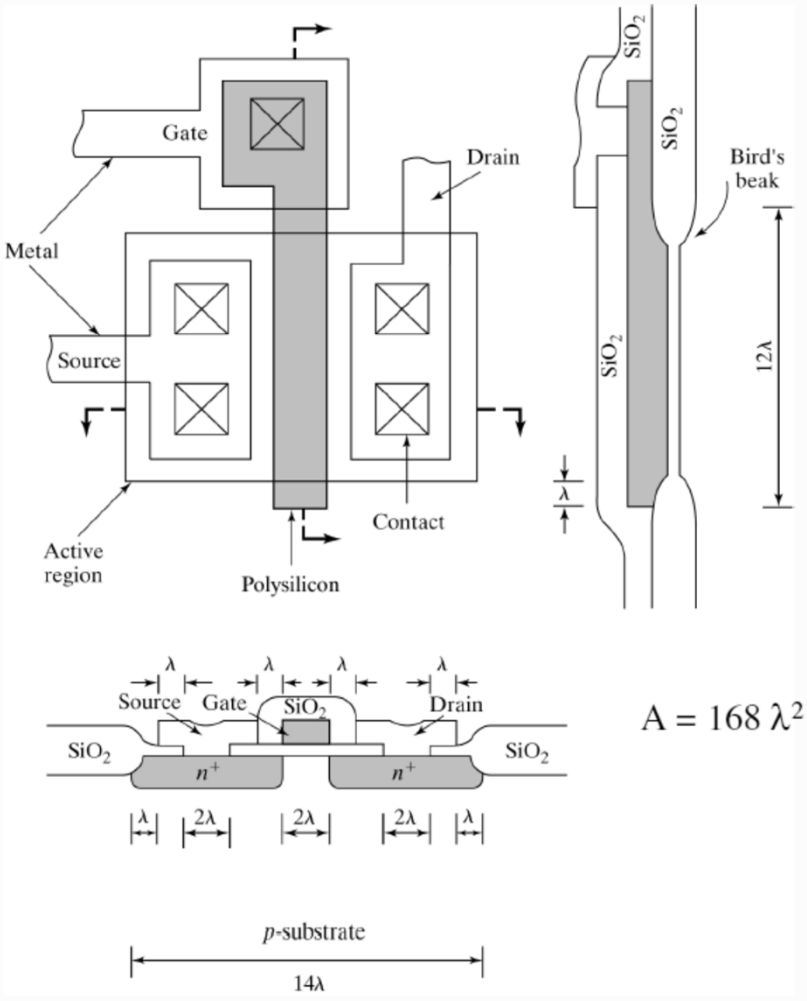
Metal Gate (Classical, but currently used)



- Metal-gate transistor layout with W/L = 5/1 using design rules from Fig. 9.11
- Total area is 416 λ^2
- Channel area is 20 λ^2 (< 5%)

Figure 9.12

Poly-Si Gate for Self-align

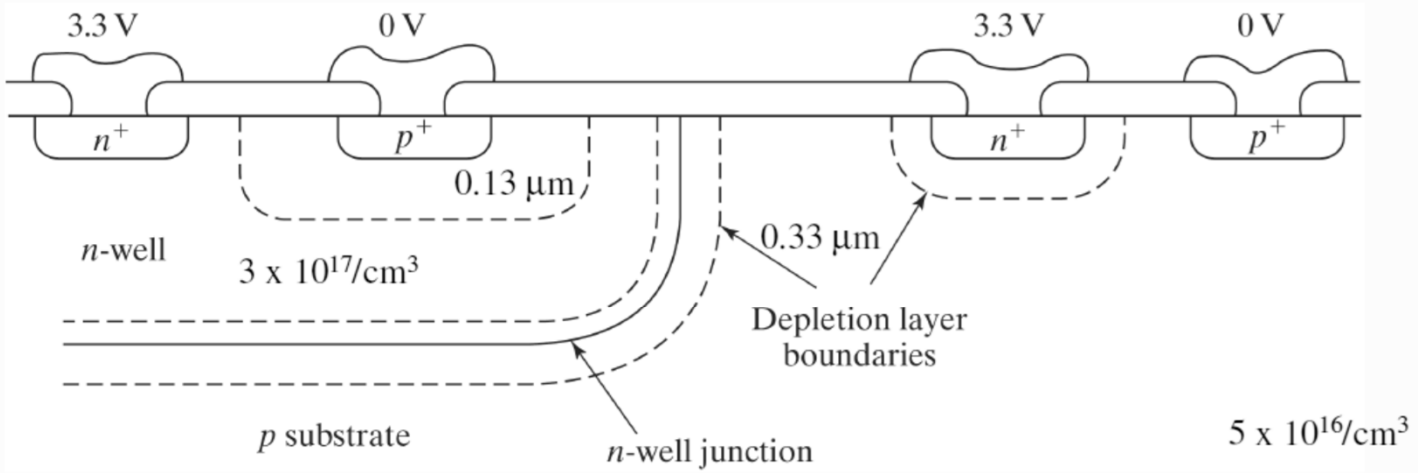


$A = 168\,\lambda^2$

- Polysilicon-gate transistor layout with W/L = 5/1 using design rules from Fig. 9.11
- Total area is $168\,\lambda^2$
- Channel area is $20\,\lambda^2$ (12%)

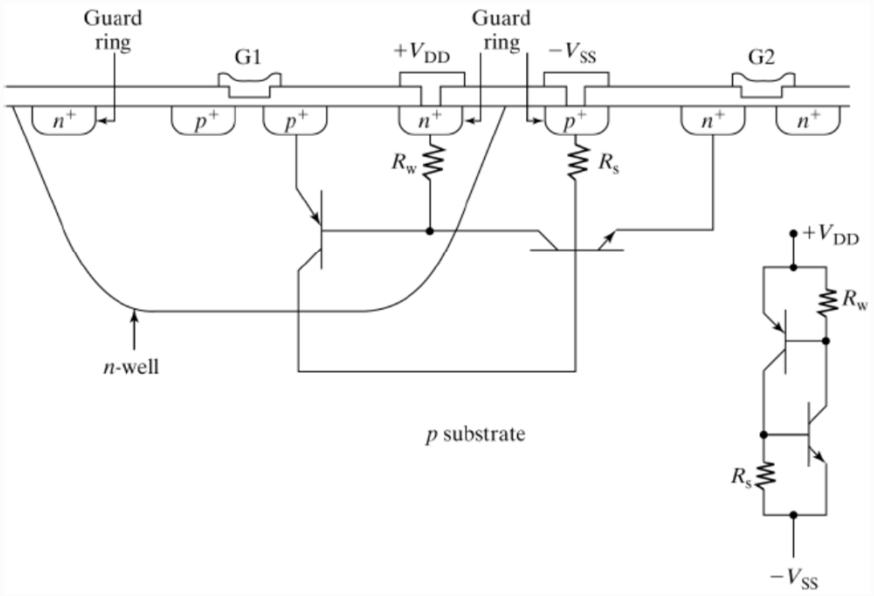
Figure 9.13

Electrical Isolation Issue



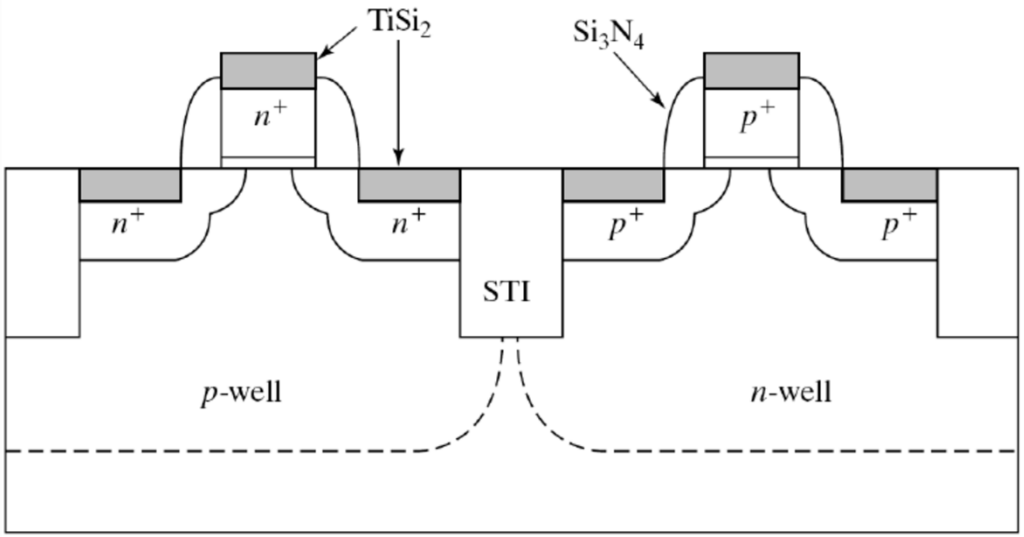
- Figure 9.17 - Minimum spacing required to ensure isolation in an n-well CMOS process
- From Ex. 9.4 in the book, the minimum spacing is
  - 0.33µm + 0.33µm + 0.13µm = 0.79 µm
- Use a spacing of 1 µm to include a safety margin

Latch-up



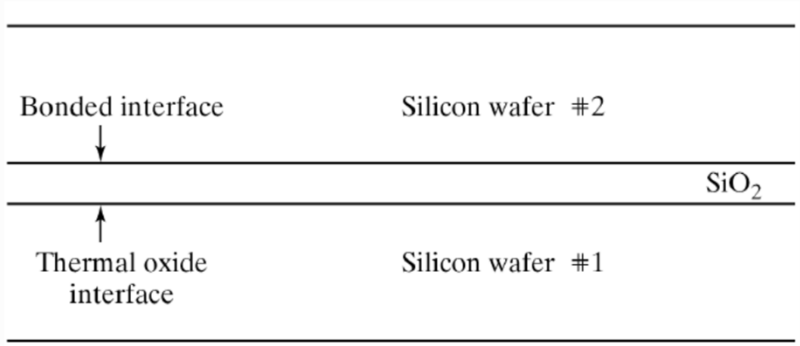
- The four layer pnpn structure used in CMOS can operate as an SCR if the bias conditions are right
- If the SCR is triggered into conduction, the “latchup” condition, then destructive currents can occur
- Must be avoided by proper biasing and device design

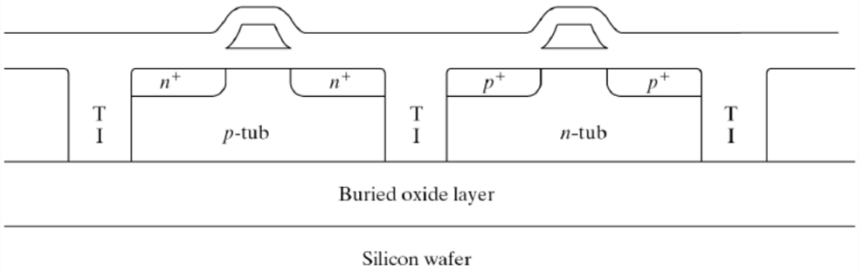
STI for minimizing Latch-up



- Shallow trench isolation in a twin-well process
- Intercepts depletion layers permitting tighter spacing
- Reduces the chance of latchup

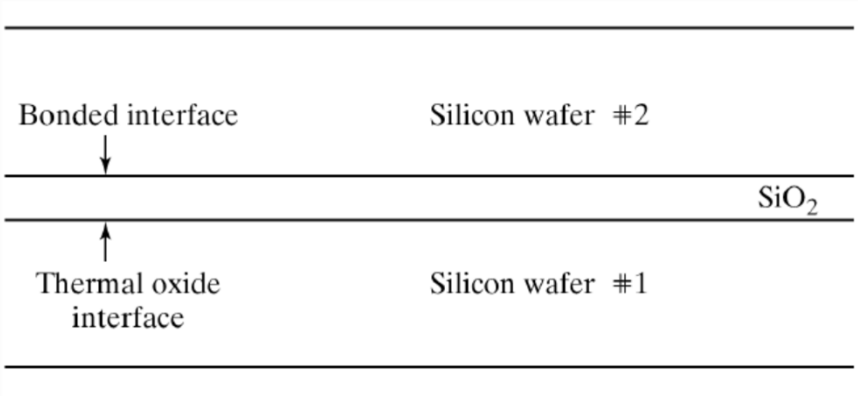
Silicon-on-Insulator (SOI) for a better isolation and V_{th} reduction





- Two wafers can be bonded together to form silicon on insulator material
- Deep oxygen implantation can be used to create a buried oxide layer (SIMOX)

Silicon-on-Insulator (SOI) for a better isolation and V_{th} reduction



- Two wafers can be bonded together to form silicon on insulator material
- Deep oxygen implantation can be used to create a buried oxide layer (SIMOX)